AMC121

Intel® Core™ 2 Duo Processor AdvancedMC™ Module Hardware Manual

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Document Revision History

Date	Explanation of changes
July 07, 2008	Initial Production Release
October 21, 2008	Updated Table 4-1, “IPMI/PICMG Command Subset Supported by the MMC Firmware,” on page 48. Updated upper CPU temperature thresholds in Table , “Table 4-4 lists the sensors that are monitored by the MMC. Note that the sensor IDs are local to the MMC. The MMC’s SDRs are inherited by the next level of management (µTCA MCMC or AMC carrier IPMC) and sensor IDs are reassigned.,” on page 52. Updated Web links.
March 19, 2009	Added caution and warning about product handling in “Safety” on page 88.
June 10, 2009	Standardized “Module Management Controller” on page 24, “Serial I/O” on page 25, and Chapter Chapter 4, “System Monitoring and Alarms.”. Updated “Memory Configuration” on page 36, “DDR SDRAM Connector” on page 76, and “Battery Backup Characteristics” on page 82 to indicate that memory and batteries are not field servicable items. Removed “Balcony Board Switch” topic. Added caution to “Balcony Board” on page 31 and “Balcony Interface Connector” on page 76 and added notes to Figure 5-1, “Connector Locations,” on page 71 and Figure 5-3, “Connector Locations (Balcony),” on page 77. Changed name of SW2 to Multifunction Swich and clarified “SW2-3 (Position 3) - Spread Spectrum Clock (SSC)” on page 40. Expanded “USB CD/DVD” on page 44. Corrected board height specification on page 83.
October 2, 2009	Standardized Chapter Chapter 9, “Agency Approvals” on page 87.
December 1, 2009	Updated “SW2-2 (Position 2) - FCLKA Configuration” on page 40 to reflect new default setting. Corrected note in “SW2-4 (Position 4) - MMC Serial Access / Serial Port” on page 41. Corrected “MMC Sensors” on page 52. Added topic “Power On Reset” on page 79.
February 2, 2011	Rebranded and reformatted entire document. Updated “Payload Shutdown Timeout” on page 60.

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Symbol Conventions in This Manual

The following symbols appear in this document:

Caution:
There is risk of equipment damage. Follow the instructions.

Warning:
Hazardous voltages are present. To reduce the risk of electrical shock and danger to personal health, follow the instructions.

Caution:
Electronic components on printed circuit boards are extremely sensitive to static electricity. Ordinary amounts of static electricity generated by your clothing or work environment can damage the electronic equipment. It is recommended that anti-static ground straps and anti-static mats are used when installing the board in a system to help prevent damage due to electrostatic discharge.

Additional safety information is available throughout this guide and in the topic “Safety” on page 88.

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Chapter 1

About This Guide

This manual describes the operation and use of the AMC121 Intel® Core™ 2 Duo Processor AdvancedMC™ Module (referred to as AMC121 in this guide). The following outline describes the focus of each chapter.

Chapter 2, “Introduction,” provides an overview of the AMC121 and includes information such as module features, functional block diagram, and a brief description of each block.

Chapter 3, “Getting Started,” provides setup information such as unpacking the module, system requirements, and installation procedures.

Chapter 4, “System Monitoring and Alarms,” describes the commands supported by the on-board Module Management Controller.

Chapter 5, “Connectors,” provides connector location, description, and pinout information for the AMC121’s AdvancedMC card edge connector, front panel and internal connectors. It also includes a description of the serial cable recommended for use with the front panel RJ11 serial connector.

Chapter 6, “Reset,” describes the AMC121 reset types with their respective sources.

Chapter 7, “Specifications,” contains mechanical, electrical, and environmental specifications as well as product reliability specifications.

Chapter 8, “Thermal Considerations,” describes the thermal requirements to reliably operate an AMC121 processor module.

Chapter 9, “Agency Approvals,” presents agency approval and certification information.

Chapter 10, “Data Sheet Reference,” provides information on data sheets, standards, and specifications for the technology designed into the AMC121.

The AMC121 assembly should be used in conjunction with the Performance Technologies software package that you have chosen, for example NexusWare® Core.

The most current documentation to support any additional components that you purchased from Performance Technologies is available at www.pt.com under the product you are inquiring about.

For additional documentation references see Chapter 10, “Data Sheet Reference.”

Text Conventions

Conventions in This Guide describes the text conventions that are used in this guide.

Conventions in This Guide

Convention	Used For
`Monospace font`	Monospace font represents sample code.
Bold font	Bold font represents: • paths • file names • UNIX commands • user input.
Italic font	Italic font represents: • notes that supply useful advice • supplemental information • referenced documents.

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Chapter 2

Introduction

This chapter provides a brief introduction to the AMC121 64-bit Intel Core 2 Duo™ AdvancedMC™ Module. It includes a product definition, a list of product features, a figure showing the AMC121 front panel, a functional block diagram, and a description of each block. Unpacking, initial board configuration and other setup information are provided in Chapter 3, “Getting Started.”

Key topics in this chapter include:

- “Product Definition” on page 19
- “AMC121 Features” on page 19
- “AMC121 Functional Blocks” on page 21
- “Software” on page 33

Product Definition

The AMC121 is a 64-bit AdvancedMC (AMC) single board compute module, featuring the Intel Core 2 Duo dual core 1.5 GHz processor, designed for high-performance embedded applications. The board incorporates the Intel 3100 integrated northbridge/southbridge chipset, supporting a 667 MHz front-side bus interface, 400 MHz 64-bit PC2-3200 DDR2 memory interface. 64-bit PC2-3200 DDR SDRAM up to 4GB is supported.

Support for a mini SD/SDHC card is provided to add local storage functionality for autonomous OS boot, file storage, etc.

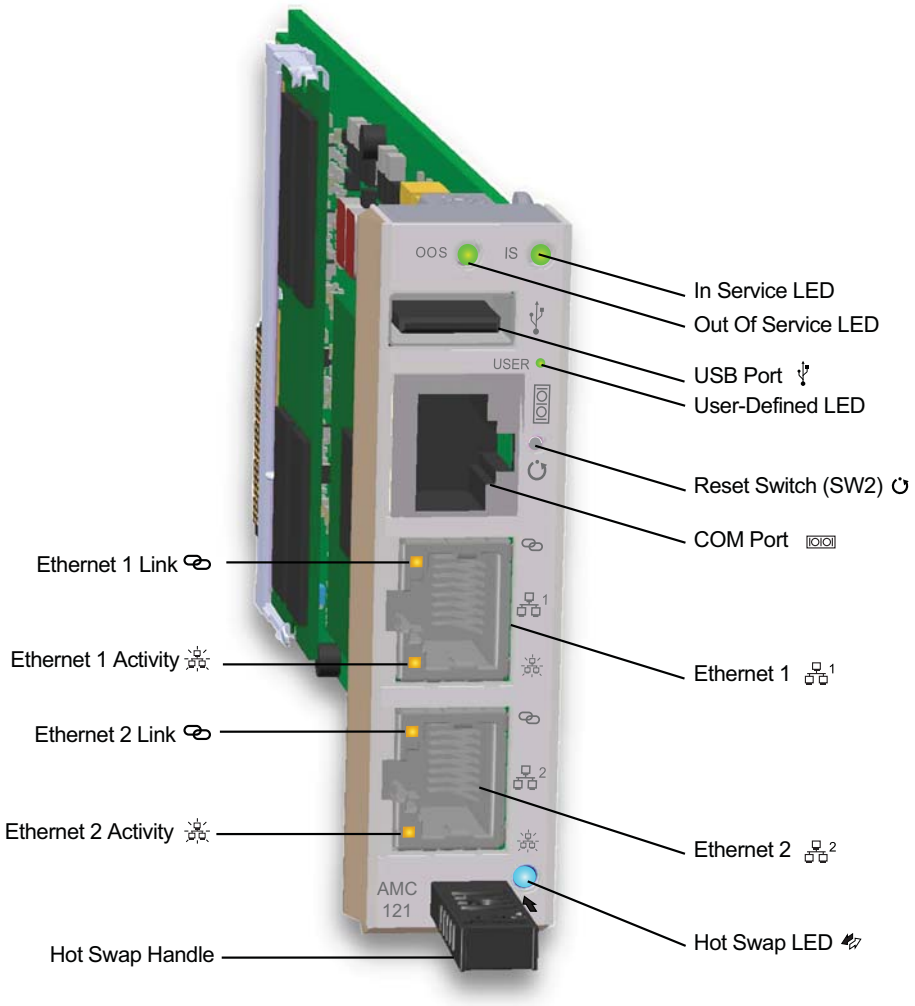
AMC121 Features

- Single, mid-size PICMG AMC.0 processor module
- PICMG AMC.0, R 2.0 compliant
- IPMI v1.5 specification compliant
- 1.5 GHz dual core Intel Core 2 Duo processor (L7400)
- Intel 64 architecture
- Supports Intel Architecture with Dynamic Execution
- PC2-3200 DDR2 400 MHz memory controller interface
- 32KB Level 1 instruction cache (per core)
- 32KB Level 1 data cache (per core)
- Up to 4MB Level 2 shared cache with Advanced Transfer Cache Architecture
- 667 MHz, Source-Synchronous FSB
- Intel Virtualization Technology
- Execute Disable Bit support for enhanced security
- System management bus

- Card edge interface contains two SATA channels, eight-lane PCI Express bus, and dual SERDES 1Gb/2.5Gb Ethernet channels
- Intel 3100 Chipset
- Dual 10/100/1000 Mb/s Ethernet links are available on the front panel via RJ45 connectors
- Supports up to 4GB of PC2-3200 DDR2 SDRAM with ECC in one 200-pin SODIMM socket
- Performance Technologies' Embedded BIOS (AMI core) stored in local flash memory
- Supports Windows® XP, Linux®, and Solaris™ 9/10 64-bit operating systems
- IPMI interface on the AMC connector
- Standard AT® peripherals include:
  - Real-time clock/CMOS RAM
  - 16C550 RS-232 serial port
  - USB 2.0 port
- Dual-stage watchdog timer
- Push-button reset switch
- LEDs:
  - USER LED, dual color (green/yellow) accessible through an I/O port address
  - Hot Swap (Blue/Off)
  - Front Panel Ethernet Link (Green)
  - Front Panel Ethernet Traffic (Flashing Yellow)

Front Panel

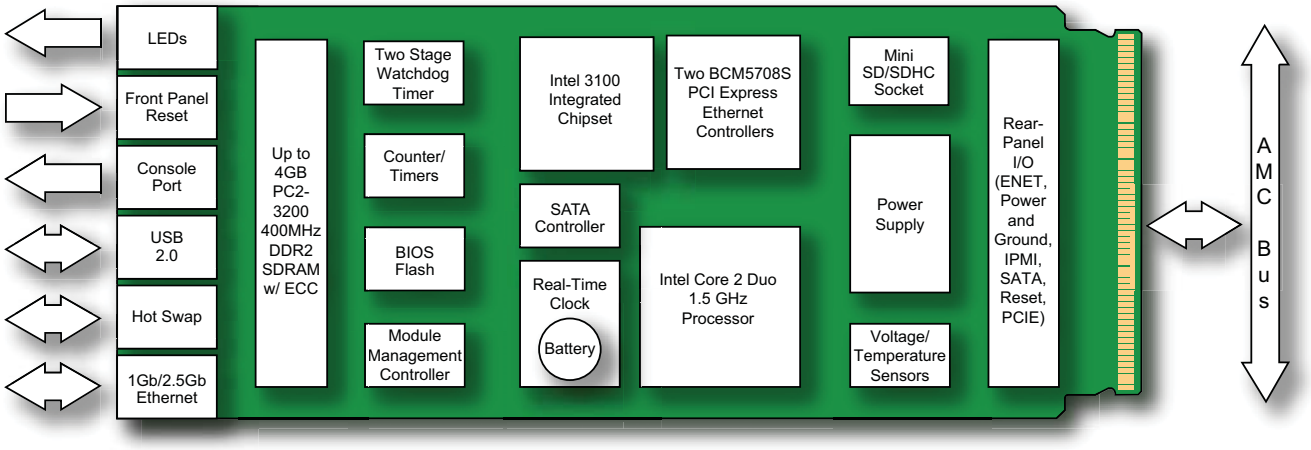
Figure 2-1: AMC121 Front Panel



AMC121 Functional Blocks

Figure 2-2 on page 22 is a functional block diagram of the AMC121. The topics following the figure provide overviews of the functional blocks.

Figure 2-2: AMC121 Functional Block Diagram



Processor

The AMC121 incorporates the Intel Core 2 Duo L7400 processor. The Intel Core 2 Duo L7400 processor is a 1.5 GHz, 17W (TDP), high performance, low power, 64-bit processor that is compatible with 32-bit applications, enabling a single architecture across 32- and 64-bit environments.

The Intel Core 2 Duo implements dual-core technology that puts two mobile-optimized execution cores in a single processor that is designed to increase performance with significant power savings. Each core can complete up to four full instructions simultaneously using an efficient 14-stage pipeline. The two cores share 4MB of L2 cache, offering more efficient data sharing, providing enhanced performance, responsiveness and power savings. Each core utilizes enhanced Intel Speedstep technology on each core independently to coordinate power-management state transitions and help save power. The 667 MHz front-side bus provides a high-speed interconnect with the Intel 3100 chipset.

The topic “Processor” on page 91 contains a link to additional information for this device.

Chipset

The AMC121 incorporates the Intel 3100 integrated chipset. The Intel 3100 chipset integrates the traditional north/south bridge functions as well as some SuperI/O and peripheral IC features into a single IC. The Intel 3100 features:

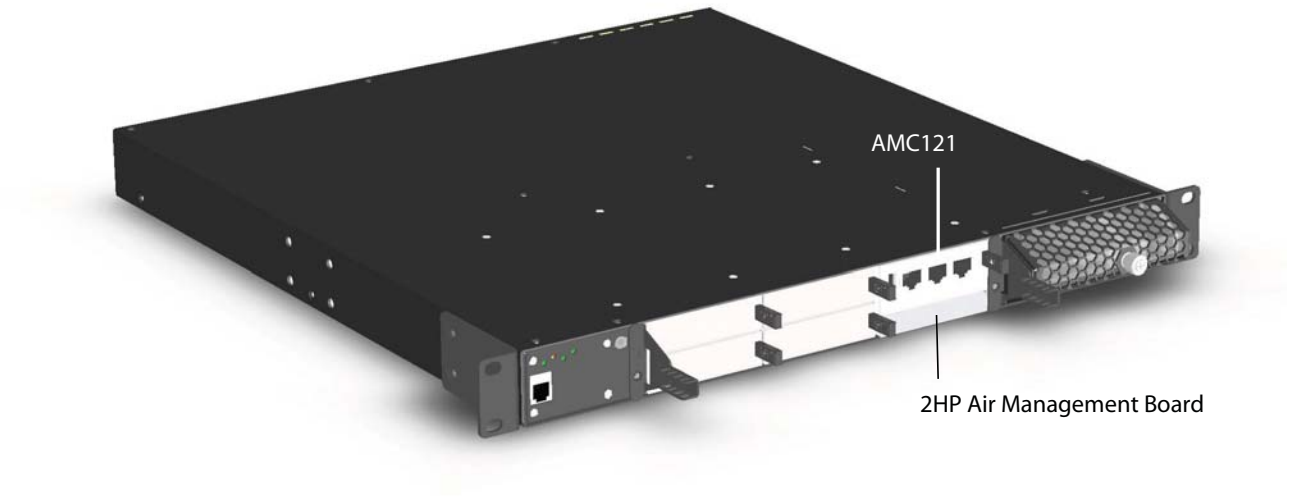
- Processor/Host bus support:
  - 64-bit, 667 MHz front side bus interface
  - Up to 36-bit host interface addressing support
  - Dynamic bus inversion to minimize power consumption on the data interface
  - In-Order Queue (IOQ) depth of 12, with debug support for the one-deep non-pipelined mode
  - Two outstanding DEFER cycles supported
  - AGTL+ driver technology with parallel termination

- Memory Interface
  - Support for dual rank, registered EDD DIMM with ECC
  - Support for 15-bit address bus, 72-bit data bus (64-bit data plus 8-bit ECC)
  - Support for base DDR2 clock rate of 200 MHz: data interface double-pumped to 400 MT/s, data bandwidth of 3.2 GB/s
  - Support for 512 Mb, 1 Gb, and 2 Gb DRAM densities
  - Support for DDR2 DIMMs using x4 or x8 DRAM technology
  - Aggressive page-close policy with one-deep, look-ahead to minimize occurrence of page-miss accesses in favor of page-empty
  - Support for standard SEC-DED (72, 64) ECC
  - Support for automatic read retry on uncorrectable errors
  - Hardware ECC auto-initialization of all populated DRAM devices under software control. Includes pre-selected hardware pattern based memory test on programmable regions.
- PCI-Express interface features:
  - The x8 interface is capable of bifurcation into two logically independent x4 interfaces with full specification compliance at half the bandwidth capability
  - Low latency, high bandwidth
  - 32-bit CRC protection on all packets
  - CRC errors are recoverable by retransmission
  - Supports 64-bit addressing
  - Advance error detection and error transmission on destination bus
  - Integrated bit-error generation and monitor function
  - PCI-E v1.0 and 1.0a compliant
  - Statistics for SNMP MIB II, Ethernet like MIB, and Ethernet MIB (802.3z, Clause 30)

AMC Interface

AMC121 is compliant with the *AdvancedMC™ Advanced Mezzanine Card Base Specification, PICMG® AMC.0 R2.0*. It is designed to be hot swappable into a mid-size bay on an AdvancedMC or MicroTCA® carrier such as Performance Technologies' AMP5070 1U MicroTCA Platform. See Figure 2-3, "AMC121 Modules Installed in an AMP5070 1U MicroTCA Platform."

Figure 2-3: AMC121 Modules Installed in an AMP5070 1U MicroTCA Platform



It can also function in a non-hot swap AMC system. Its AdvancedMC card edge connector provides rear I/O connectivity to the AdvancedMC bus in accordance with the AMC Type 4 spec. It includes:

- Two 10/100/1000/2500Mb SerDes Ethernet ports
- Serial ATA (SATA)

See “AdvancedMC Card Edge Connector” on page 72 for more information. Chapter 10, “Data Sheet Reference,” contains links to the PICMG Web site, where the specification may be obtained.

Module Management Controller

The AMC121 includes a Module Management Controller (MMC) based on the Atmel ATMEGA128L-8MU, which interfaces to the local Intelligent Platform Management bus (IPMB-L). The MMC monitors and controls the module’s payload per the PICMG AMC.0 specification.

See Chapter 4, “System Monitoring and Alarms,” on page 47 for more information on MMC functionality, supported commands, AMC121 sensors, and the firmware upgrade process.

The AMC121 is compliant with standard Intelligent Platform Management Interface v1.5 Specification functionality. See “Module Management Controller” on page 92 for information about this specification.

Memory

The AMC121 includes one 200-pin, Small Outline Dual In-line Memory Module (SODIMM) socket that can be populated with up to 4GB DDR2 ECC Registered SDRAM. The BIOS automatically determines the SDRAM's size and speed.

Universal Serial Bus (USB)

The Universal Serial Bus (USB) provides a common interface to many peripherals such as keyboard, serial ports, and mouse ports. The AMC121 supports booting from USB devices, such as CD-ROM or floppy.

The AMC121 supports one standard USB 2.0 port, available at the front panel. See Figure 2-1, “AMC121 Front Panel,” on page 21.

The AMC121's USB resides in the Intel 3100 chipset. The topic “Chipset” on page 91 provides a link to the data sheet for this device. Connector locations and pinouts are documented in the topic “USB Connector” on page 75.

Serial I/O

On its front panel, the AMC121 includes one 6-pin RJ11 serial port connector with RS232 signal levels and 15 KV ESD protection. See Figure 2-1, “AMC121 Front Panel,” on page 21. Due to the limited number of pins in the RJ11 connector, hardware flow control is unavailable. This port is pinned out for Data Terminal Equipment (DTE) operation. Request-to-send (RTS), clear-to-send (CTS), and modem-control signals are not supported. This connector is shared by COM1 on the payload and the serial debug interface on the MMC. Switch SW2-4 is used to select which serial port is routed to the front panel connector. See “Multifunction Switch (SW2)” on page 40 for more information.

The AMC121 payload includes two 16C550, PC-compatible serial ports. When configured appropriately, COM1 is available for general use at the RJ11 connector on the front panel. COM1 supports data transfers at speeds up to 115.2 Kb/sec with BIOS support. The baud rate for BIOS supported console redirection defaults to 9600 and is set in the BIOS setup utility. See “BIOS Configuration Overview” on page 42 for more information about BIOS setup. For COM1 port pinout information, see “COM1 Serial Port” on page 74.

COM2 is dedicated to communication with the payload serial interface on the MMC. See “Serial Interface Subsystem” on page 53 for more information about serial communication with the MMC. The default baud rate for COM2 is 9600 and is set in the BIOS setup utility. Note that the baud rate of COM2 must match the baud rate of the payload serial interface on the MMC.

Caution:
Be careful to insert the RJ11 connector on the management cable into the serial port only. Inserting it into an Ethernet connector may damage the Ethernet connector pins. See Figure 3-3, “RJ11 Cable Connection,” on page 39.

SATA Interface

The AMC121 includes an integrated Serial ATA (SATA) controller that routes two independent SATA interfaces, each of which is SATA 1.0 compliant, to the AdvancedMC edge connector. An AdvancedMC and MicroTCA carrier that support SATA capability, such as the Performance Technologies AMC570 Video/Storage AdvancedMC Module with Audio and AMP5070 1U MicroTCA Platform, can provide connectivity for AMC SATA drives.

The AMC121's SATA controller resides in the Intel 3100 chipset. The topic “Chipset” on page 91 provides a link to the data sheet for this device. The AdvancedMC edge connector location and pinout are documented in “AdvancedMC Card Edge Connector” on page 72.

Ethernet Interface

The AMC121 includes two BCM5708S PCI Express Ethernet controllers that route two independent SerDes Ethernet interfaces to the AMC edge connector. These two Ethernet controllers are intended for high-performance network applications, with each including the following features:

- 10/100/1000/2500 Mbps SerDes Ethernet ports routed to the AMC connector. This enables interfacing to other AMC cards on the same carrier or interfacing with a hub/switch on a carrier.
- iSCSI controller (providing for offload/acceleration as well as iSCSI boot support, etc.)
- Large on-chip memories
- RDMA controller
- Other performance features such as TCP/IP/UDP checksum, TCP segmentation, etc.
- TCP/IP offload engine
- Advanced network features

Although the hardware supports TOE and iSCSI, these features are not enabled by default. Contact your Performance Technologies sales representative if you are interested in enabling these features.

The topic “Ethernet” on page 91 contains links to the product brief for the Broadcom BCM5708S Ethernet controllers used onboard the AMC121. AMC connector location and pinout are documented in “AdvancedMC Card Edge Connector” on page 72.

Real-Time Clock, CMOS RAM and Battery

The real-time clock performs timekeeping functions and includes 256 bytes of battery-backed CMOS RAM in two banks that are reserved for BIOS use. Timekeeping features include a time-of-day clock and a multi-century calendar with alarm features and century rollover. The time, date, and CMOS values can be specified or returned to their defaults by using the BIOS setup program. See the topic “BIOS Configuration Overview” on page 42 for more information.

Note: *The recommended method of accessing the date in systems with Performance Technologies processor modules is indirectly from the real time clock via the BIOS. The BIOS on Performance Technologies processor modules contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the real time clock during each BIOS request (INT 1Ah) to read the date and, if less than 80 (1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.*

Two rechargeable button-cell batteries located on the AMC121 power the real-time clock and CMOS memory when the AMC121 is not powered externally. The battery is intended for AC power fails only and has an estimated life of 60 days (with batteries fully charged). It recharges whenever standby power is present.

The AMC121's real-time clock resides in the Intel 3100 chipset. The topic “I/O Controller” on page 92 provides a link to more information for this device.

Reset

The AMC121 provides the following reset types:

- Power on reset
- Backend power down
- Push button resett
- NMI

See Chapter 6, “Reset,” for more information.

Two-Stage Watchdog Timer

The watchdog timer optionally monitors system operation and is programmable for one of eight different timeout periods (from 1µs to 1050s). It is a two-stage watchdog, meaning that it can be enabled to produce an SERIRQ, NMI or SMI interrupt during the first stage followed by a system reset for the second stage. Failure to strobe the watchdog timer within the programmed time period may result in an NMI/SMI/SERIRQ, a system reset, or both. A register bit is set if the watchdog timer caused the reset event.

The AMC121's two-stage watchdog timer resides in the Intel 3100 chipset. The topic “Chipset” on page 91 provides a link to the datasheet for this device.

Counter/Timers

Three counter/timers as defined for the PC/AT® are included on the AMC121. Operating modes supported by the counter/timers include:

- Interrupt on count
- Frequency divider
- Square wave generator
- Software triggered
- Hardware triggered “one shot”

The AMC121's 8254-compatible counter/timer resides in the Intel 3100 chipset. The topic “Chipset” on page 91 provides a link to the datasheet for this device.

LED Indicators

The LEDs located on the front panel are defined below. See Figure 2-1, “AMC121 Front Panel,” on page 21.

Front Panel Ethernet (RJ45 Connector)

- Green = Link (top)
- Flashing yellow = Activity (bottom)

Out of Service (OOS), In Service (IS)

These LEDs are used to indicate an “out of service” condition or an “in service” status, per the *PICMG Advanced Mezzanine Card AMC.0 Specification R2.0*. Although these LEDs are managed by the MMC, a carrier manager or shelf manager can override the MMC's local LED settings.

The OOS LED is activated to indicate that the payload is known to be out of service (payload power is off, held in reset, or faulted in a way that precludes operation). Otherwise the OOS LED is off. The health of the board cannot be inferred solely from the state of this LED. The default local color of the OOS LED is determined by FRU data and is configurable as either red or amber. Contact Performance Technologies Customer Support for information about configuring this color.

The IS LED is activated when the OOS LED is turned off. It is never turned on when the OOS LED is on. The IS LED is green when all sensors are within the critical thresholds or amber when one or more sensors have exceeded a critical threshold.

Hot Swap

The Hot Swap LED indicates the module's state as it deactivates in preparation for extraction or reactivates after insertion. See the PICMG AMC.0 specification for more information. A link is available in the topic “PICMG Specifications” on page 92.

Insertion Sequence

- Off = module handle open. Management power is not enabled.
- Blue on = module is fully seated in carrier. Module's management power is enabled. User may initiate activation by pushing in the handle on the module's front panel to close the hot swap switch.
- Blue long blink = module handle is closed. Module is being activated.
- Off = module handle is closed. Module is in normal operational state.

Extraction Sequence

- Off = module is in normal operational state. User may initiate deactivation by pulling out the module handle to open the hot swap switch, sending a request via the MMC to the carrier for a hot swap extraction.
- Blue short blink = module handle open. Module is waiting to be deactivated. Not safe to extract module.
- Blue on = module is quiesced, module payload power is disabled. Safe to extract module.

User-Defined

One bicolored, user-defined LED (Green/Amber/Off). See the topic “Programming the LEDS” on page 45 for more information.

Board Status LEDs

Board status LEDs (located as SMT LEDs on the PCB. These are for debug/status):

D19: Payload power supply good signal

- On = power good on main payload power rails
- Off = power supplies not within spec

D23: SATA activity indicator. This indicator is the logical “OR” of both SATA channels out the AMC edge connector. This LED indicates activity on either of the SATA channels.

- On = SATA access
- Off = no SATA access

D11: Not used.

D8: Ethernet “B” (SerDes out the AMC edge connector) 2.5Gb link indication

- On = 2.5Gb link
- Off = no 2.5Gb link

D10: Ethernet “B” (SerDes out the AMC edge connector) 1Gb link indication

- On = 1Gb link
- Off = no 1Gb link

D12: Ethernet “B” PCIe data link layer status

- On = PCIe data link layer is active
- Off = not active

D13: Ethernet “B” PCIe link up status

- On = PCIe link
- Off = no PCIe link

D16: Ethernet “B” power status

- On = power good
- Off = power not good

D9: Not used.

D17: Ethernet “A” (SerDes out the AMC edge connector) 2.5Gb link indication

- On = 2.5Gb link
- Off = no 2.5Gb link

D15: Ethernet “A” (SerDes out the AMC edge connector) 1Gb link indication

- On = 1Gb link
- Off = no 1Gb link

D14: Ethernet “A” PCIe data link layer status

- On = PCIe data link layer is active
- Off = not active

D7: Ethernet “A” PCIe link up status

- On = PCIe link
- Off = no PCIe link

D18: Ethernet “A” power status

- On = power good
- Off = power not good

Rear-Panel I/O

The AMC121 transitions the following I/O signals through the AMC card edge connector to the carrier:

- 10/100/1000/2500Mb SerDes Ethernet
- IPMI
- RESET
- Power and Ground
- SATA
- X8 PCI Express

See the topic "AdvancedMC Card Edge Connector" on page 72 for more information.

Balcony Board

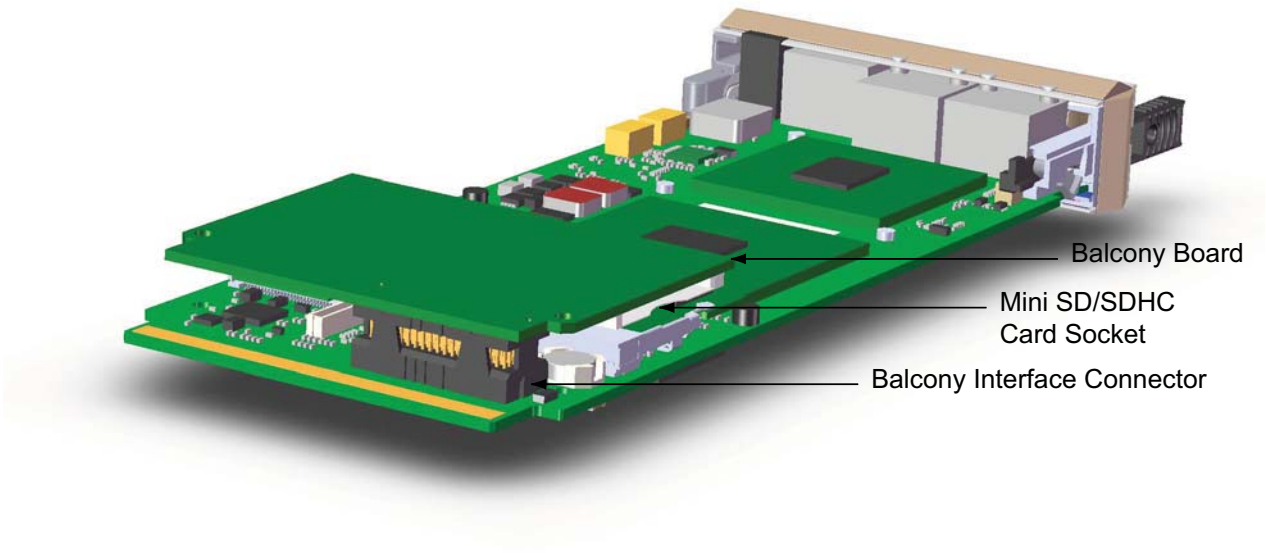
An XMC style connector provides the interface between the AMC121 and a balcony board that provides additional functionality, including:

- Dual 1Gb Ethernet interfaces supporting the front panel RJ45 connectors
- Mini SD/SDHC card socket (supports SD 2.0 specification)

See Figure 2-4 and the topic "Balcony Interface Connector" on page 76 for more information.

Caution:
Do not attempt to remove the balcony board from the AMC121. Doing so will void your warranty.

Figure 2-4: AMC121 with Balcony Board



Ethernet Interfaces (Balcony Board Based)

In addition to the two SerDes Ethernet channels on the baseboard, the AMC121 provides an additional two 10/100/1000Base-T Ethernet channels through the Intel 82571EB GbE controller located on the balcony board. The two onboard Ethernet channels are accessible via two front panel RJ45 connectors. See Figure 2-1, “AMC121 Front Panel,” on page 21. These connectors each have two LEDs to indicate the status of each channel.

The topic “Ethernet” on page 91 contains links to the data sheets for the Intel 82571EB GbE controller used onboard the AMC121. Connector locations and pinouts are documented in “Ethernet Connectors” on page 75.

Mini SD/SDHC Card Socket

Mini SD card support is provided via a mini SD card socket located on the balcony board. See Figure 5-3, “Connector Locations (Balcony),” on page 77, for the socket location. The SD/SDHC card socket is SD 2.0 specification compliant.

Software

BIOS

The Performance Technologies Embedded BIOS (AMI core) is user-configurable to boot an operating system from one of the following locations:

- USB mass storage device (floppy, hard drive, CD-ROM drive, disk key (flash), etc.)
- Serial ATA (SATA) hard drives
- Ethernet (PXE)
- Any add-on cards/boards that support a BIOS boot specification option ROM

Operating Systems Supported

- WinXP and WinXP 64 have been installed and successfully run through Microsoft's Hardware Compatibility Test (HCT).
- Solaris 10 has been installed successfully. Upon successful completion of Sun Hardware Compatibility Test Suite (HCTS), results will be posted to Sun's Web pagehttp://www.sun.com/bigadmin/hcl/overview.html.
- Red Hat Enterprise Linux AS 4 Update 3 (32 and 64 bit versions) has been installed successfully.
- Nexusware Core has been installed and successfully run through Performance Technologies' validation test suite.

IPMI

For more information about how to program software to interact with the IPMI firmware, refer to the *Intelligent Platform Management Interface v1.5 Specification* and the *Intelligent Platform Management Interface Implementer's Guide*. A link to these publications is available in the topic “Module Management Controller” on page 92.

Chapter 3

Getting Started

This chapter summarizes the information you need to make the AMC121 operational. Please read it before attempting to use the board.

Key topics in this chapter include:

- “Unpacking” on page 36
- “Electrical and Environmental Requirements” on page 36
- “Memory Configuration” on page 36
- “I/O Configuration” on page 38
- “Connectivity” on page 39
- “Switches” on page 40
- “BIOS Configuration Overview” on page 42
- “Installing the Operating System” on page 43
- “Programming the LEDS” on page 45
- “Optimizing AMC121 Performance” on page 45

Unpacking

Check the shipping carton for damage. If the shipping carton and contents are damaged, notify the carrier and Performance Technologies for an insurance settlement. Retain the shipping carton and packing material for inspection by the carrier. Obtain authorization before returning any product to Performance Technologies. Refer to “Customer Support and Services” on page 16 for assistance information.

Warning:
Like all equipment that uses MOS devices, the AMC121 must be protected from static discharge. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with your order when handling the module.

Electrical and Environmental Requirements

Electrical specifications are presented in detail in “Electrical and Environmental Specifications” on page 81.

The AMC121 is supplied with a heat sink that allows the processor to operate between 0° and approximately 55°C ambient with a minimum of 300 LFM (1.27 meters per second) of external airflow. It is the user's responsibility to ensure that the AMC121 is installed in a chassis capable of supplying adequate airflow. The maximum power dissipation of the processor is 25W. External airflow must be provided at all times. See Chapter 7, “Specifications,” and Chapter 8, “Thermal Considerations,” for more details.

Warning:
Operating the AMC121 without adequate airflow will damage the processor.

The AMC121 may contain materials that require regulation upon disposal. Please dispose of this product in accordance with local rules and regulations. For disposal or recycling information, please contact your local authorities or the Electronic Industries Alliance at http://www.eiae.org/.

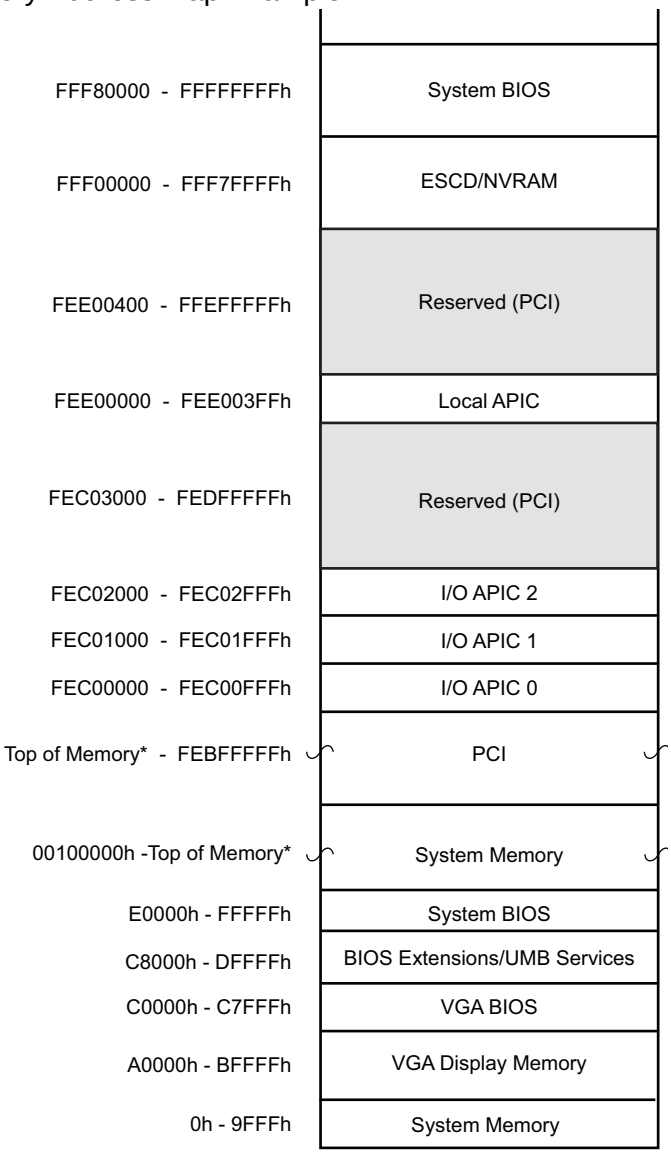
Memory Configuration

The AMC121 is populated with PC2-3200 ECC DDR2 SDRAM located on one registered, 200-pin SO-RDIMM socket. The socket supports up to 4GB, 400 MHz DDR2-400 (PC2-3200) memory modules with ECC.

Figure 3-1, “Memory Address Map Example,” on page 37, shows an example of memory addressing for the AMC121.

Memory is not a field serviceable item. Return the module to Performance Technologies for memory replacement. See “Return Merchandise Authorization (RMA)” on page 17 for more information about returning merchandise.

Figure 3-1: Memory Address Map Example



Note: **This address varies depending on how much RAM is installed and how much address space is required by PCI devices. The default PCI address base is 3GB. If the amount of installed RAM is less than the PCI address base this will be the top of physical memory. If more RAM is installed this will be the PCI address space base address and system memory will continue above 4GB up to the top of memory.*

I/O Configuration

The AMC121 addresses up to 64 KB of I/O using a 16-bit I/O address.

The AMC121 is populated with many of the most commonly used I/O peripheral devices for industrial control and computing applications. The I/O address location for each of the peripherals is shown in Figure 3-2.

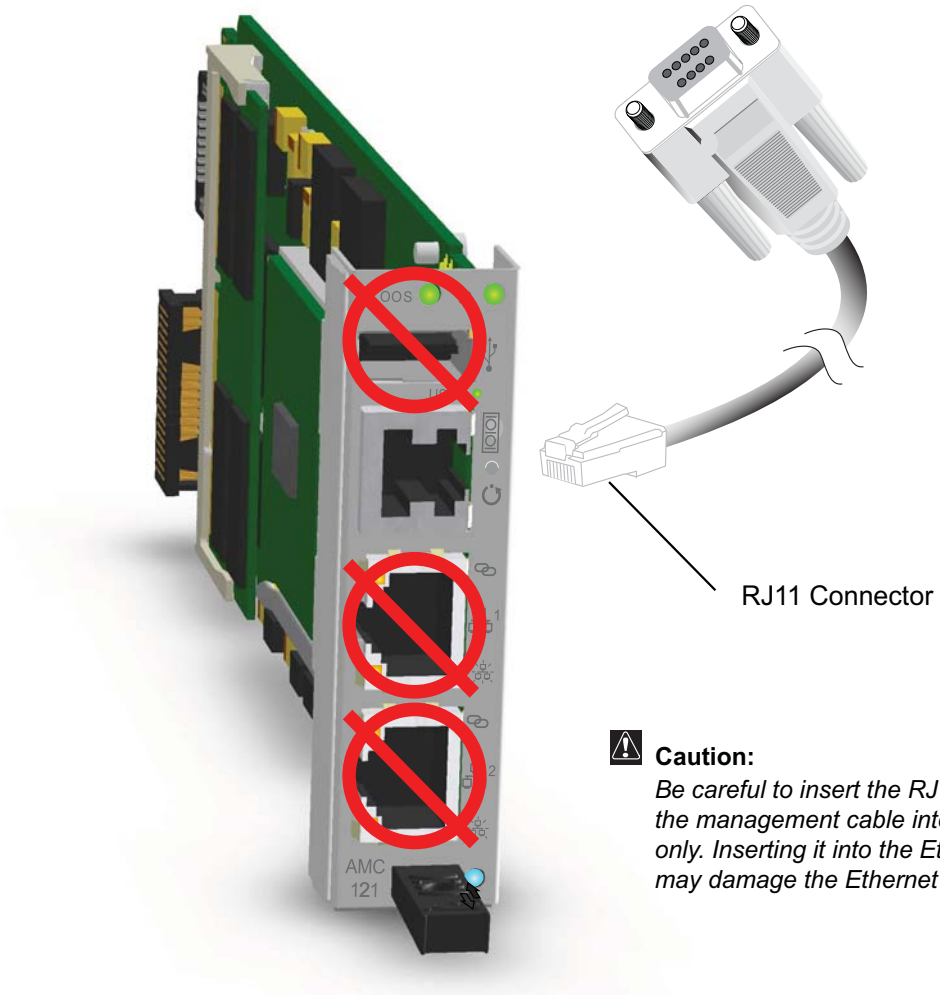
Figure 3-2: I/O Address Map

CFCh	PCI Configuration Data Register (double word)
CF9h	Reset Generator
CF8h	PCI Configuration Index Register (double word)
500h	Chipset GPIO Base
540h	Chipset SMB Base
400h	Chipset Power Management Base
E1-E8h	AMC121 System Registers
C0 – DFh	On-board Slave DMA Controller
A0 - A1h	On-board Slave Interrupt Controller
94 – 9Fh	DMA Controller
92h	Fast Gate A20/Reset Control
81 - 90h	On-board DMA Page Registers
78 - 80h	AMC121 System Registers
70 - 77h	NMI Enable/RTC Controller
64h	PS/2 Keyboard/Mouse
60h	PS/2 Keyboard/Mouse
4Fh	SIO IO Data (Write Only)
4Eh	SIO IO Index (Write Only)
40 - 43h	On-board Timer/Counters
2Fh	IPMC IO Data
2Eh	IPMC IO Index
20 - 21h	On-board Master Interrupt Controller
0 - 1Fh	On-board Master DMA Controller

Connectivity

The AMC121 provides several connectors for interfacing to application specific devices. Refer to Chapter 5, “Connectors,” for complete connector descriptions and pinouts.

Figure 3-3: RJ11 Cable Connection



Caution:
Be careful to insert the RJ11 connector on the management cable into the Serial port only. Inserting it into the Ethernet connector may damage the Ethernet connector pins.

Switches

Front Panel Switches

Push-Button Reset (SW1)

The AMC121 provides a push-button reset switch on its front panel. When the system reset button is pressed, the AMC121 resets itself. See Figure 2-1, “AMC121 Front Panel,” on page 21.

Hot Swap Switch (SW3)

The AMC121 provides a hot swap handle on its front panel. See Figure 2-1, “AMC121 Front Panel,” on page 21. This handle is attached to a mechanical latching mechanism and to the hot swap switch. When this switch opens or closes it sends a request via the MMC to the carrier for a hot swap extraction or insertion. Its function and behavior is defined by the PICMG AMC.0 specification. See the topic “PICMG Specifications,” on page 92, for a link to this publication. The hot swap LED indicates the state of the module during extraction and insertion. See the topic “LED Indicators,” on page 27, for more information.

Multifunction Switch (SW2)

SW2 is a four-position, single pole DIP switch pack. See Figure 3-4, “CMOS Reset and COM1 Port Redirection Switch Location,” on page 41, for the switch position on the AMC121.

SW2-1 (Position 1) - BIOS CMOS Reset

To reset CMOS settings to the BIOS defaults, move SW2-1 from the OFF position (default) to the ON position briefly and then return the switch to the OFF position.

SW2-2 (Position 2) - FCLKA Configuration

Setting SW2-2 to OFF configures the AMC121 to receive the PCIe clock (FCLKA) from the backplane regardless of e-keying commands. Use this setting in AMC.1 R1.0 carriers.

Setting SW2-2 to ON (default) configures the AMC121 to source/receive/isolate the PCIe clock (FCLKA) based on ekeying commands in compliance with AMC.1 R2.0.

If the AMC121 does not boot up when powered on, it is likely that FCLKA is not configured properly for the specific carrier. For more information about configuring FCLKA on this AMC, please contact Performance Technologies' Customer Support (see “Customer Support and Services” on page 16).

SW2-3 (Position 3) - Spread Spectrum Clock (SSC)

Setting SW2-3 to OFF (default) disables the spread spectrum feature of the clock generator when the payload is powered up.

Setting SW2-3 to ON enables the spread spectrum feature of the clock generator when the payload is powered up.

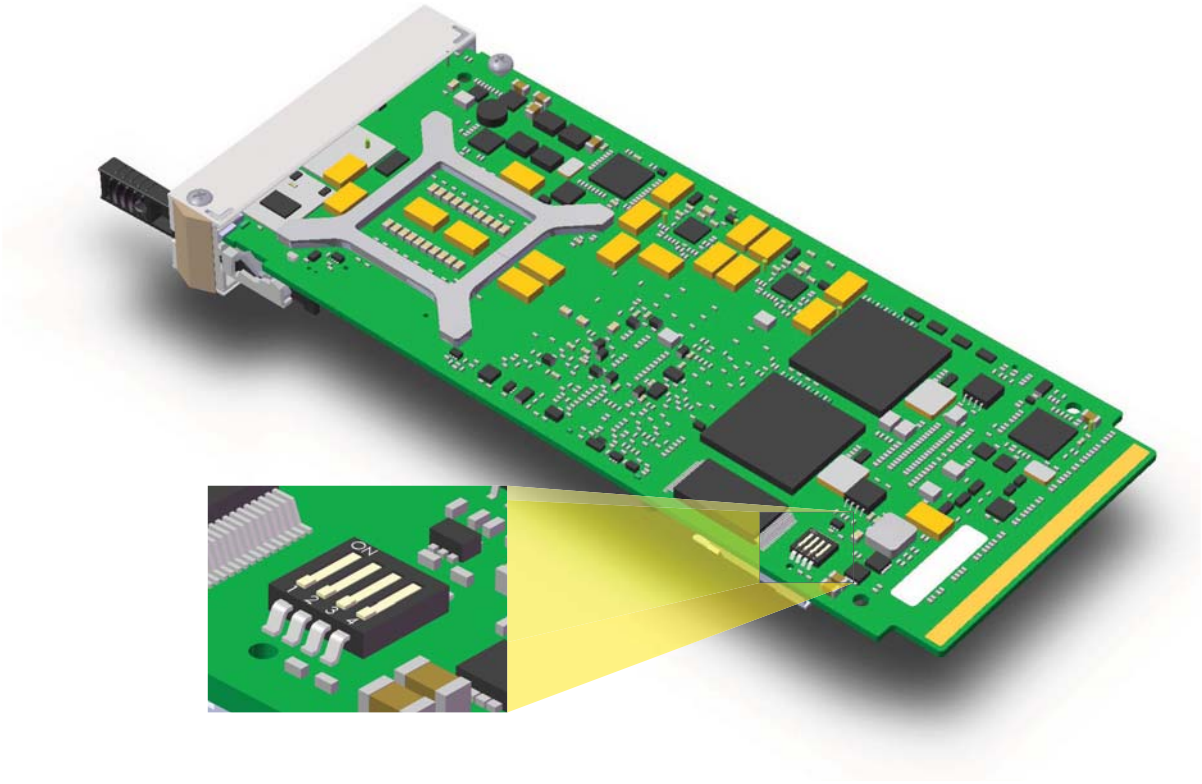
Note: *Enabling SSC is allowed only when FCLKA is not being received from the backplane. Therefore, to enable SSC, SW2-2 and SW2-3 must be set to ON and ekeying must not require the AMC121 to receive FCLKA*.

SW2-4 (Position 4) - MMC Serial Access / Serial Port

Setting SW2-4 to ON provides serial access to the MMC through the front panel RJ11 COM1 port connector. See Figure 2-1, “AMC121 Front Panel,” on page 21. Setting SW2-4 to OFF (default) causes the connector to operate as a PC-compatible serial port.

Note: *On power-up, with SW2-4 in the OFF position, the MMC briefly displays information before the COM1 serial communications begin. With this switch in the OFF position the serial port continues to be connected to the MMC until the payload processor is powered up and starts its boot process. Once the payload processor begins its boot routine the serial port is switched to the payload processor. If payload power is subsequently turned off or payload is held in reset then console returns to MMC.*

Figure 3-4: CMOS Reset and COM1 Port Redirection Switch Location



BIOS Configuration Overview

The Performance Technologies Embedded BIOS has many separately configurable features. These features are selected by running the built-in setup utility. The system configuration settings are saved in a portion of the battery-backed RAM (CMOS) in the real-time clock device and are used by the BIOS to initialize the system at boot-up or reset. The configuration is protected by a checksum word for system integrity.

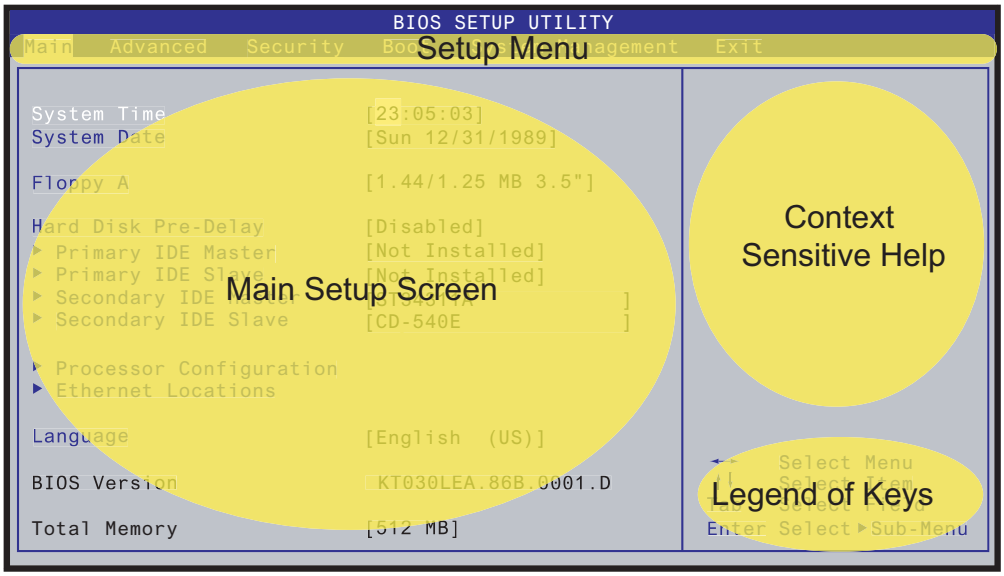
To access the setup utility, press the **F2** key during the POST test and initialization at boot time. Setup runs once the POST functions complete.

When Setup runs, an interactive configuration screen displays. See Figure 3-5, “Setup Screen Layout” for an example. Setup parameters are divided into different categories. The available categories are listed in a menu across the top of the setup screen. The parameters within the highlighted (current) category are listed in the main (left) portion of the setup screen. Context-sensitive help is displayed in the right portion of the screen for each parameter. A legend of keys is listed at the bottom of the setup screen.

Use the left and right arrow keys to select a category from the menu. Use the up and down arrow keys to select a parameter in the main portion of the screen. Use the **+** or **-** keys or press the **Enter** key to open a list of selections to change the value of a parameter.

Items in the main portion of the screen that have a triangular mark to their left are submenus. To display a submenu, use the up and down arrow keys to highlight the submenu and then press the **Enter** key.

Figure 3-5: Setup Screen Layout



Console Redirection

Console redirection allows users to monitor the AMC121's boot process and to run the AMC121's BIOS setup utility from a remote serial terminal. Connection is made directly through the serial port.

The console redirection feature is most useful in cases where it is necessary to communicate with the AMC121 in an embedded application without video support.

Console redirection is configurable from the AMC121's BIOS setup utility Remote Access Configuration setup menu under the Advanced tab on the main menu.

The default CMOS settings within the Remote Access Configuration menu are as follows.

Remote Access:	Enabled
Serial Port Number:	COM1
Base Address, IRQ:	3F8h, 4
Serial Port Mode:	09600 8,n,1
Flow Control:	None
Redirection After BIOS POST:	Always
Terminal Type:	VT100
VT-UTF8 Combo Key Support:	Disabled

Notes: *Because an RJ11 connector is used for the front panel serial port, hardware flow control is not supported. The only options for flow control are None and Software Control.*

Some operating systems may have problems with the redirection if BIOS POST is set to Always. If there is a problem, try either the Disabled or Boot Loader options.

Installing the Operating System

For more detailed information about your operating system, refer to the documentation provided by the operating system vendor and to the Performance Technologies Web site.

To install the operating system:

1. Install peripheral devices. AMC devices are automatically configured by the BIOS during the boot sequence.
2. Most operating systems require initial installation on a hard drive from a USB CD/DVD or PXE. These devices should be configured, installed, and tested with the supplied drivers before attempting to load the new operating system.
3. Read the release notes and installation documentation provided by the operating system vendor. Be sure to read any readme files or documents provided with the OS as these typically note documentation discrepancies or compatibility problems.
4. Select the appropriate boot device order in the setup boot menu depending on the OS installation media used. To boot from a USB CD-ROM, first connect the USB drive, then enter the BIOS setup utility and move the “CD-ROM” device to the top of the boot list (or above any other bootable devices). To boot a USB Floppy, connect the floppy device to the board, then enter the BIOS setup utility, move “Removable Devices” to the top of the boot order on the Boot screen, and then move the USB floppy device to the top of the removable devices list.

5. Proceed with the OS installation as directed, being sure to select appropriate device types if prompted. Refer to the appropriate hardware manuals for specific device types and compatibility modes of Performance Technologies products. A link to Performance Technologies manuals is available in the topic “User Documentation,” on page 92.
6. When installation is complete, reboot the system and set the boot device order in the setup boot menu.

Note: *For more information about the BIOS setup utility, see the topic “BIOS Configuration Overview,” on page 42.*

USB CD/DVD

Note: *Win XP and Red Hat Enterprise Linux AS 4 Update 3 (AMD64/Intel EM64T) have been validated for this installation.*

To run the BIOS setup utility with a bootable OS installation CD or DVD in an external USB drive:

1. Cable an external USB CD/DVD drive to the USB port on the AMC121.
2. Ensure the USB CD/DVD drive is powered on.
3. Insert the bootable OS installation CD/DVD into the drive.
4. Run the AMC121 BIOS setup utility by hitting the F2 key while the SBC is booting up.
5. Ensure that the USB device is listed in the Boot Devices and is above any other device that may have a bootable OS image (i.e. hard drive).
   a. Use the right arrow key to highlight the *Boot* category in the setup menu. The Boot Settings information appears in the main setup screen.
   b. Arrow down to *Boot Device Priority* and press <Enter>. The boot order list appears and the top position in the boot order is highlighted.
   c. Press <Enter>. A dialogue box with a list of boot devices appears.
   d. Arrow up or down to highlight the USB device. Press <Enter>. *USB* appears at the top of the Boot Device Priority list.
   e. Press <Esc> to exit to the main menu.
   f. Right arrow to select the *Exit* menu item. Save *Changes and Exit* is highlighted.
   g. Press <Enter>. *OK* is highlighted.
6. Press <Enter> to exit the BIOS setup utility.

PXE

The AMC121 BIOS settings default to attempt PXE boot. If this feature is not to be used, the BIOS settings can be changed so the PXE boot attempt is skipped. This speeds the BIOS boot sequence.

Creating a bootable PXE OS or installing an OS over PXE is beyond the scope of this manual.

Operating Systems Supported

WinXP and WinXP 64 have been installed and run through Microsoft's Hardware Compatibility Test (HCT) successfully.

Solaris 10 has been installed successfully (pending). Upon successful completion of Sun Hardware Compatibility Test Suite (HCTS), results will be posted to Sun's Web page http://www.sun.com/bigadmin/hcl/overview.html.

Red Hat Enterprise Linux AS 4 Update 3 (32 and 64 bit versions) has been installed successfully. Upon successful completion of Red Hat Enterprise Certification Test Suite, the results will be posted on the Red Hat Web site http://hardware.redhat.com

Programming the LEDS

The AMC121 includes one user-controlled, bicolor (amber/green) LED located on the front panel. See Figure 2-1, “AMC121 Front Panel,” on page 21. The user LED is software programmable through GPIO bits 24 and 25 of the Intel 3100 GPIO_USE_SEL1 register (500h). The LED is turned off after a power cycle or a reset.

As shown below, two bits each are used to control the state of the user LED. Since a bicolor LED is used, there are four states for the LED: amber, green, both colors off and both colors on.

	STATE			
Bit	Amber	Green	Both Off	Both On
Bit 24	0	1	1	0
Bit 25	1	0	1	0

The GPIO bits that control the user LED's bits are in the same register as other system critical functions. It is important not to change the state of other bits in this register when modifying the user LED status.

Optimizing AMC121 Performance

Intel and AMD processors run x86 code and are generally compatible when it comes to running software. However the internal architecture is different between different Intel processors and different AMD processors. To maximize overall performance of the different CPUs it is important to specify which CPU the code will be executing on when compiling it.

Many operating systems detect the CPU type upon installation and load the appropriate modules to optimize operating system performance.

See the topic “Processor,” on page 91, for more optimization guidelines.

Chapter 4

System Monitoring and Alarms

Introduction

The AMC121 performs system monitoring and alarming functions using the flexible, industry standard, Intelligent Platform Management Interface (IPMI). The AMC121 comes equipped with an on-board Module Management Controller (MMC) chip, IPMI and IPMB J-connector pinouts, and MMC firmware already installed on the board. The MMC firmware is based on Pigeon Point System's (PPS) MMC firmware. Some of the functions available on this board through the IPMI interface include:

- Monitoring of the CPU and board temperatures with critical and non-critical alerting
- Monitoring of the voltage rails with critical and non-critical alerting
- Remote reset and shutdown of the board
- Monitoring of ejector switches for hot swap functionality: Performance Technologies NexusWare IPMI driver and firmware provide features for hot swap
- Monitoring and event reporting of critical errors
- Interface to IPMB line (IPMB-L)

In order to take advantage of the features provided by the firmware, IPMI-aware applications must be developed. Information on IPMI v1.5 is provided at http://www.intel.com/design/servers/ipmi/spec.htm. Key topics in this chapter include:

- "MMC Functions," on page 47
- "Summary of Supported Commands," on page 48
- "Device Locator Record," on page 50
- "Sensors," on page 52
- "Serial Interface Subsystem," on page 53
- "Firmware Upgrade Process," on page 61

MMC Functions

The MMC performs system monitoring and alarming functions using the flexible, industry standard, Intelligent Platform Management Interface (IPMI). The module comes equipped with an on-board MMC and IPMI v1.5 firmware already installed on the module. The MMC firmware is based on Pigeon Point System®'s (PPS) MMC firmware. Some of the functions available on the module through the IPMI interface include:

- Monitoring of the CPU and board temperatures with critical and non-critical alerting
- Monitoring of the voltage rails with critical and non-critical alerting
- Remote reset and shutdown of the module (hard and soft)
- Monitoring of ejector switches for hot-swap functionality (Performance Technologies' NexusWare IPMI driver and firmware provide additional payload features for hot swap)
- Monitoring and event reporting of critical errors

- Fabric and clock e-keying
- Interface to local IPMB (IPMB-L)

In order to take advantage of the features provided by the firmware, IPMI-aware applications must be developed. Information on IPMI v1.5 is provided at:

http://www.intel.com/design/servers/ipmi/spec.htm

Summary of Supported Commands

Table 4-1, "IPMI/PICMG Command Subset Supported by the MMC Firmware," lists all the commands supported by the MMC.

The **Spec Ref** column indicates where in the relevant specification a command is defined. IPMI references are to v1.5 unless indicated otherwise. The **MMC Req** column indicates if a particular command is required by the relevant specification (*AMC Specification* or *HPM.1 Specification*) or is optional. See the various notes under the table for more information.

Table 4-1: IPMI/PICMG Command Subset Supported by the MMC Firmware

Command	Spec Ref	NetFn	CMD	MMC Req
IPM Device "Global" Commands				
Get Device ID	17.1	App	01h	Mandatory
Cold Reset	17.2	App	02h	Optional
Warm Reset	17.3	App	03h	Optional
Broadcast "Get Device ID"[a]	17.9	App	01h	Mandatory
Messaging Commands				
Set BMC Global Enables	18.1	App	2Eh	Mandatory
Get BMC Global Enables	18.2	App	2Fh	Mandatory
Clear Message Flags	18.3	App	30h	Mandatory
Get Message Flags	18.4	App	31h	Mandatory
Get Message	18.6	App	33h	Mandatory
Send Message	18.7	App	34h	Mandatory
BMC Watchdog Timer				
Reset Watchdog Timer	21.5	App	22h	Mandatory
Set Watchdog Timer	21.6	App	24h	Mandatory
Get Watchdog Timer	21.7	App	25h	Mandatory
Event Commands				
Set Event Receiver	23.1	S/E	00h	Mandatory
Get Event Receiver	23.2	S/E	01h	Mandatory
Platform Event (a.k.a. "Event Message")	23.3	S/E	02h	Mandatory
Sensor Device Commands				
Get Device SDR Info	29.2	S/E	20h	Mandatory
Get Device SDR	29.3	S/E	21h	Mandatory
Reserve Device SDR Repository	29.4	S/E	22h	Mandatory
Get Sensor Reading Factors	29.5	S/E	23h	Optional

Table 4-1: IPMI/PICMG Command Subset Supported by the MMC Firmware (Continued)

Command	Spec Ref	NetFn	CMD	MMC Req
Set Sensor Hysteresis	29.6	S/E	24h	Optional
Get Sensor Hysteresis	29.7	S/E	25h	Optional
Set Sensor Threshold	29.8	S/E	26h	Optional
Get Sensor Threshold	29.9	S/E	27h	Optional
Set Sensor Event Enable	29.10	S/E	28h	Optional
Get Sensor Event Enable	29.11	S/E	29h	Optional
Get Sensor Event Status	29.13	S/E	2Bh	Optional
Get Sensor Reading	29.14	S/E	2Dh	Mandatory
FRU Device Commands				
Get FRU Inventory Area Info	28.1	Storage	10h	Mandatory
Read FRU Data	28.2	Storage	11h	Mandatory
Write FRU Data	28.3	Storage	12h	Mandatory
AdvancedTCA Commands				
Get PICMG Properties	3-10	PICMG	00h	Mandatory
FRU Control	3-25	PICMG	04h	Mandatory
FRU Control Capabilities	3-24	PICMG	1Eh	Mandatory
Get FRU LED Properties	3-27	PICMG	05h	Mandatory
Get LED Color Capabilities	3-28	PICMG	06h	Mandatory
Set FRU LED State	3-29	PICMG	07h	Mandatory
Get FRU LED State	3-30	PICMG	08h	Mandatory
Get Device Locator Record ID[b]	3-35	PICMG	0Dh	Mandatory
AMC Commands				
Set AMC Port State	3-26	PICMG	19h	Optional/ Mandatory
Get AMC Port State	3-27	PICMG	1Ah	Optional/ Mandatory
Set Clock State	3-44	PICMG	2Ch	Optional/ Mandatory
Get Clock State	3-45	PICMG	2Dh	Optional/ Mandatory
HPM.1 Upgrade Commands (HPM.1)				
Get Target Upgrade Capabilities	3-3	PICMG	2Eh	Mandatory
Get Component Properties	3-5	PICMG	2Fh	Mandatory
Abort Firmware Upgrade	3-15	PICMG	30h	Optional
Initiate Upgrade Action[c]	3-8	PICMG	31h	Optional/ Mandatory
Upload Firmware Block	3-9	PICMG	32h	Mandatory
Finish Firmware Upload	3-10	PICMG	33h	Mandatory
Activate Firmware	3-11	PICMG	35h	Mandatory
Query Self-Test Results[d]	3-12	PICMG	36h	Optional/ Mandatory
Query Rollback Status[e]	3-13	PICMG	37h	Optional/ Mandatory
Initiate Manual Rollback[f]	3-14	PICMG	38h	Optional/ Mandatory

a. See "Device ID" below, for the device ID data retrieved in response to a **(Broadcast) Get Device ID** command for this module.

b. See "Device Locator Record" below, for the IPMB management controller device locator record retrieved in response to a **Get Device Locator Record ID** command for this module.
c. The HPM.1 **Initiate Upgrade Action** command is mandatory for an IPM Controller indicating that any of its implemented components supports preparation for Firmware Upgrade or comparison of the current firmware
d. The HPM.1 **Query Self-test Results** command is mandatory for IPM Controllers indicating self-test is supported in the Self-test capabilities field of the "Get target upgrade capabilities" response or the Self-test capabilities field of the Upgrade Image header.
e. The HPM.1 **Query Rollback Status** command is mandatory for IPM Controllers supporting automatic or manual Roll-back.
f. The HPM.1 **Manual Firmware Rollback** command is mandatory for IPM Controllers indicating manual firmware Rollback is supported in the *Manual firmware Rollback* capabilities field of the "Get target upgrade capabilities" response.

Device Locator Record

The MMC firmware supports the *Get Device Locator Record ID* command for FRU device #0 (the only FRU device represented by an MMC). The MMC firmware obtains the ID of the IPMB management controller device locator record by scanning the SDR records embedded into the firmware.

Table 4-2 shows an example of an IPMB management controller device locator record (SDR type 0x12) describing the properties of the MMC:

Table 4-2: IPMB Management Controller Device Locator Record

Parameter	Value
Power State Notification	
ACPI System Power State notification required	NO
ACPI Device Power State notification required	NO
Global Initialization	
Controller logs Initialization Agent errors	NO
Log Initialization Agent errors accessing this controller	NO
Event Generation	Enable event message generation from controller
Device Capabilities	
Chassis Device	NO
Bridge	NO
IPMB Event Generator	YES
IPMB Event Receiver	NO
FRU Inventory Device	YES
SEL Device	NO
SDR Repository Device	NO
Sensor Device	YES
FRU Entity ID	0xC1
Entity Instance	(slot dependent)
OEM-specific	0
Device ID String Type/Length	8-bit ASCII with size of Device ID String (see below)
Device ID String	AMC121

Device ID

The MMC firmware provides the following device ID data in response to the (Broadcast) *Get Device ID* command:

Table 4-3: MMC Device ID

Parameter	Value
Device ID	0x00
Provides Device SDRs	YES
Device Revision Number	0x00
Device Available	YES
Firmware Revision	Changes with each release
IPMI Version	1.5
Additional Device Support	
Chassis Device	NO
Bridge	NO
IPMB Event Generator	YES
IPMB Event Receiver	NO
FRU Inventory Device	YES
SEL Device	NO
SDR Repository Device	NO
Sensor Device	YES
Manufacturer ID	0x000614
Product ID	0x0009
Auxiliary Firmware Revision Information	0x00000000

Sensors

Table 4-4 lists the sensors that are monitored by the MMC. Note that the sensor IDs are local to the MMC. The MMC's SDRs are inherited by the next level of management (µTCA MCMC or AMC carrier IPMC) and sensor IDs are reassigned.

Table 4-4: MMC Sensors

Sensor ID	Description	Lower Non-Recoverable Threshold	Lower Critical Threshold	Lower Non-Critical Threshold	Upper Non-Critical Threshold	Upper Critical Threshold	Upper Non-Recoverable Threshold
0	Hot Swap	N/A	N/A	N/A	N/A	N/A	N/A
11	3.3V MGMT	3.0V	3.068V	3.135V	3.465V	3.533V	3.6V
13	12V	10.0V	10.4V	10.8V	13.2V	13.6V	14.0V
12	5V	4.7V	4.72V	4.74V	5.27V	5.28V	5.3V
10	3V VBAT	2.55V	2.7V	2.8V	N/A	N/A	N/A
1	1.8V	1.7V	1.72V	1.74V	1.86V	1.88V	1.9V
14	DIMM TEMP	-5°C	0°C	5°C	65°C	85°C	95°C
3	POWER GOOD	N/A	N/A	N/A	N/A	N/A	N/A
4	CPU ERROR	N/A	N/A	N/A	N/A	N/A	N/A
5	THERM TRIP	N/A	N/A	N/A	N/A	N/A	N/A
2	VCCP	0.96V	0.98V	1.0V	1.1V	1.12V	1.14V
9	CPU TEMP	-5°C	0°C	5°C	80°C	100°C	110°C
8	INLET TEMP	-5°C	0°C	5°C	60°C	80°C	N/A
6	BMC Watchdog	N/A	N/A	N/A	N/A	N/A	N/A
7	Version Change	N/A	N/A	N/A	N/A	N/A	N/A

Interpreting Sensor Events

The ATCA specification includes the following definitions for the sensor event severity levels:

- IPMI non-critical / PICMG 3.0 minor / telco minor – a warning that things are somewhat out of normal range, but not really a "problem" yet. See "Non-Critical Events" below.
- IPMI critical / PICMG 3.0 major / telco major – things are still in valid operating range, but are getting close to the edge; unit still operating within vendor-specified tolerances. See "Critical Events" below.
- IPMI non-recoverable / PICMG 3.0 critical / telco critical – unit no longer operating within vendor-specified tolerances. See "Non-Recoverable Events" below.

Non-Critical Events

Non-critical events are informative only. They do not indicate that the module is outside of its operating limits. In general, no action is required. However, in certain contexts, system or shelf management software may decide that preventive action should be taken. For example, if several modules in a shelf report upper non-critical temperature events, the shelf manager might decide to increase fan speed.

Critical Events

Critical events indicate that the module is still within its operating limits, but it is close to exceeding one of those limits. Possible action in this case is to closely monitor the alarming sensor and take more aggressive action if it approaches the non-recoverable threshold.

Non-Recoverable Events

Non-recoverable events indicate that the module may no longer be functioning because it is now outside of its operating limits. It is likely that action is required or has already been taken by the local hardware/firmware. For example, a processor may have shut itself down because its maximum die temperature was exceeded, or a shelf manager may decide to deactivate the module because the processor is too hot.

Serial Interface Subsystem

The MMC firmware implements a communication protocol over the payload and/or serial debug interfaces. The communication is in the form of formatted ASCII strings.

The Serial Interface Protocol Lite (SIPL) is based on the IPMI-defined Terminal Mode of the serial/modem interface. The following sections describe the SIPL:

- “Terminal Mode Messages and Commands,” on page 53
- “Terminal Mode Line Editing,” on page 55
- “Supported PPS Extension Commands,” on page 55

Terminal Mode Messages and Commands

Terminal Mode Message Format

Terminal Mode messages have the following format:

```
[<message data>]<newline>
```

The left bracket and the right bracket plus `<newline>` characters serve as START and STOP delimiters for a message. The MMC does not support multi-line IPMI messages.

Raw IPMI Messages

The SIPL supports raw IPMI messages that are entered as sequences of case-insensitive hex-ASCII pairs, each pair optionally separated from the previous one with a single `<space>` character. What follows are examples of raw IPMI request messages in Terminal Mode:

```
[18 00 22]<newline>
[180022]<newline>]
```

The MMC handles raw IPMI messages in the same way as it handles IPMI/PICMG/AMC messages coming from the IPMB-L bus and, with the exception that IPMI/PICMG/AMC replies are routed to the interfaces from which the respective requests have come (i.e. either the serial debug or payload interface of the MMC).

Terminal Mode Text Commands

The SIPL does not support Terminal Mode ASCII text commands defined by the *IPMI Specification (section 13.7.8)*.

Pigeon Point Systems (PPS) Extension Commands

The MMC firmware supports a set of PPS extension commands that are used to control and monitor the carrier Intelligent Platform Management Controller (IPMC) state over the serial debug interface. These commands are used to read the MMC status, implement graceful payload shutdown, etc.

The PPS extension commands are implemented as OEM IPMI commands with network function codes 2Eh/2Fh and message body transferred in the same manner as for raw IPMI messages (see "Raw IPMI Messages," on page 53). Figure 4-1, "PPS Extension Command Request," shows an example of a PPS extension command request:

Figure 4-1: PPS Extension Command Request

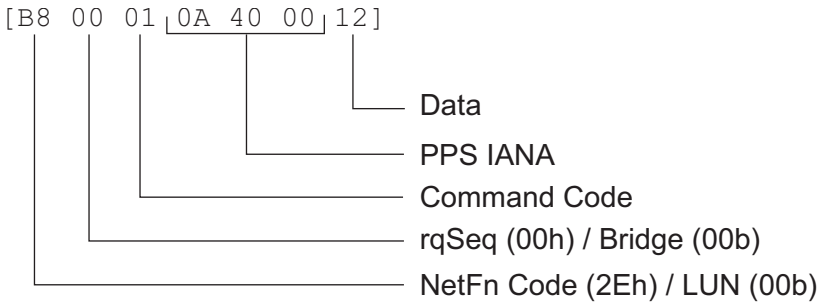
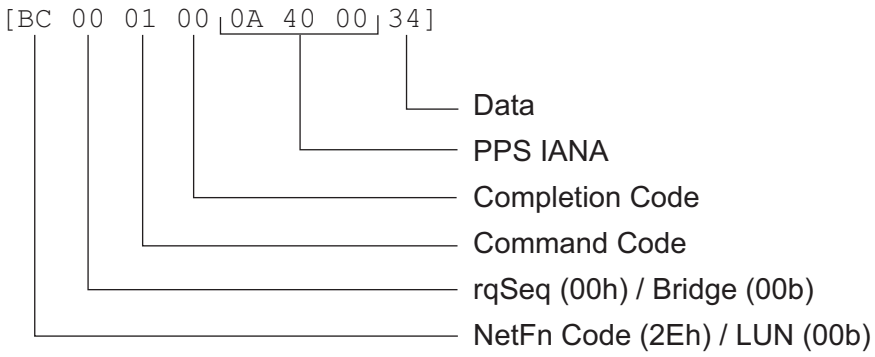


Figure 4-2, "PPS Extension Command Response," shows an example of a PPS extension command response:

Figure 4-2: PPS Extension Command Response



Terminal Mode Line Editing

The MMC does not support input line editing functionality defined as optional in the *IPMI Specification (section 13.8)*.

Supported PPS Extension Commands

The MMC firmware supports the following PPS extension commands (see "Pigeon Point Systems (PPS) Extension Commands," on page 54):

Table 4-5: PPS Extension Commands Supported by the MMC

Command Request/Response	Code	Likely Command Source(s)	Description	See Also
Get Status	0x00	Serial debug and payload interfaces	Read the MMC status	Get Status Command
Get Serial Interface Properties	0x01	Serial debug and payload interfaces	Get the properties of a serial interface	Serial Line Properties Commands
Set Serial Interface Properties	0x02	Serial debug and payload interfaces	Set the properties of a serial interface	
Get Debug Level	0x03	Serial debug interface	Get debug/verbosity level	Debug/Verbosity Level
Set Debug Level	0x04	Serial debug interface	Set debug/verbosity level	
Get Payload Communication Timeout	0x09	Serial debug and payload interfaces	Get the timeout for payload communications	Payload Communication Timeout
Set Payload Communication Timeout	0x0A	Serial debug and payload interfaces	Set the timeout for payload communications	
Graceful Reset	0x11	Payload interface	The payload is ready to be shut down/reset	Graceful Payload Reset
Diagnostic Interrupt Results	0x12	Payload interface	Return diagnostic interrupt results	Payload Diagnostic Interrupt
Get Payload Shutdown Timeout	0x15	Serial debug and payload interfaces	Get the timeout for payload shutdown	Payload Shutdown Timeout
Set Payload Shutdown Timeout	0x16	Serial debug and payload interfaces	Set the timeout for payload shutdown	
Get Geographic Address	0x2C	Serial debug and payload interfaces	Get the geographic address	Get Geographic Address Command

The MMC accepts all PPS extension commands listed in Table 4-5 from both serial interfaces, as well as IPMB-L. This is done to achieve additional flexibility and extensibility in the MMC functionality.

The PPS extension commands listed in Table 4-5 are referred to as the SIPL commands throughout this document. The following sections discuss the SIPL commands in more detail.

Get Status Command

The IPMC status is four bytes describing the logical state of the IPMC and the payload. Table 4-6, “IPMC Status Bits,” provides a description of the IPMC status bits:

Table 4-6: IPMC Status Bits

Bit	Name	Description
Byte 1		
0 (LSB)	Control	If set to 0, the IPMC control over the payload is disabled.
1-2	NA	Reserved
3	Sensor Alert	If set to 1, indicates that at least one of the IPMC sensors detects threshold crossing.
4	Reset Alert	If set to 1, indicates that the payload is going to be reset.
5	Shutdown Alert	If set to 1, indicates that the payload is going to be shut down.
6	Diagnostic Interrupt Request	If set to 1, indicates that a payload diagnostic interrupt request has arrived.
7 (MSB)	Graceful Reboot Request	If set to 1, indicates that the payload is requested to initiate the graceful reboot sequence.
Byte 2		
0-7	NA	Reserved
Byte 3		
0-7	NA	Reserved
Byte 4		
0-3	NA	Reserved
4	Message Received	If set to 1, indicates that a message for the payload has been received.
5-7	NA	Reserved

The IPMC firmware notifies the payload about changes of all status bits except for bits 0-2 of byte 1 by sending an unprintable character (ASCII 07, BELL) over the payload interface. The payload is expected to use the **Get Status** command to identify pending events and other SIPL commands to provide a response (if necessary). The event notification character is sent in a synchronous manner, and does not appear in the contents of SIPL messages sent to the payload.

The **Get Status** command has the following synopsis:

```
[B8 xx 00 0A 40 00]
```

The IPMC responds to the **Get Status** command with the following reply:

```
[BC xx 00 00 0A 40 00 <byte1> <byte2> <byte3> <byte4>]
```

Serial Line Properties Commands

The SIPL provides commands to get/set the properties of the MMC serial interfaces (the serial debug interface and the payload interface):

- "Get Serial Interface Properties Command," on page 57
- "Set Serial Interface Properties Command," on page 57

Get Serial Interface Properties Command

The **Get Serial Interface Properties** command is used to get the properties of a particular serial interface. This command has the following synopsis:

`[B8 xx 01 0A 40 00 <interface ID>]`

The `<interface ID>` parameter can have one of the values shown in Table 4-7, "The <interface ID> Parameter Values," below.

Table 4-7: The `<interface ID>` Parameter Values

Interface ID	Description
0	Serial debug interface
1	Payload interface

The MMC responds to the **Get Serial Interface Properties** command with the following reply:

`[BC xx 01 00 0A 40 00 <interface properties>]`

The `<interface properties>` parameter has the bit fields shown in Table 4-8, "The <interface properties> Parameter Bit Fields," below.

Table 4-8: The `<interface properties>` Parameter Bit Fields

Bits	Name	Description
0-3	Baud Rate ID	The baud rate ID defines the interface baud rate as follows: 0 – 9600 bps 1 – 19200 bps 2 – 38400 bps 3 – 57600 bps 4 – 115200 bps
4-6	NA	Reserved
7 (MSB)	Echo On	If this bit is set, the MMC enables echo for the given serial interface.

Set Serial Interface Properties Command

The **Set Serial Interface Properties** command is used to change the properties of a given interface:

`[B8 xx 02 0A 40 00 <interface ID> <interface properties>]`

Debug/Verbosity Level

The SIPL provides commands to enable and disable output of error/diagnostic messages to the serial debug interface at runtime:

- "Get Debug Level Command," on page 58
- "Set Debug Level Command," on page 58

Get Debug Level Command

To get the current debug level, the **Get Debug Level** command must be used. This command has the following synopsis:

`[B8 xx 03 0A 40 00]`

The MMC responds to the **Get Debug Level** command with the following reply:

`[BC xx 03 00 0A 40 00 <debug level>]`

The `<debug level>` parameter contains the bit fields shown in Table 4-9, "MMC Debug Levels," below.

Table 4-9: MMC Debug Levels

Bit	Name	Description
0 (LSB)	Error Logging Enable	If set to 1, the MMC outputs error/diagnostic messages onto the serial debug interface.
1	Low-level Error Logging Enable	If set to 1, the MMC outputs low-level error/diagnostic messages onto the serial debug interface.
2	Alert Logging Enable	If set to 1, the MMC outputs important alert messages onto the serial debug interface.
3	Payload Logging Enable	If set to 1, the MMC provides a trace of SIPL activity on the payload interface onto the serial debug interface.
4	IPMB Dump Enable	If set to 1, the MMC provides a trace of IPMB messages that are arriving to/going from the MMC via IPMB-L.
5-7	NA	Reserved

Set Debug Level Command

To change the current debug level, the **Set Debug Level** command must be used. This command has the following synopsis:

`[B8 xx 04 0A 40 00 <debug level>]`

Payload Communication Timeout

Some of the SIPL commands are subject to payload communication timeouts. If the payload does not respond with a correct reply within a definite period of time, the MMC assumes that a payload communication timeout occurred and acts accordingly. The SIPL timeout value also limits the period of time given to the payload to prepare for a payload reset.

- "Get Payload Communication Timeout Command," on page 59
- "Set Payload Communication Timeout Command," on page 59

Get Payload Communication Timeout Command

The MMC supports reading of the payload communication timeout using the **Get Payload Communication Timeout** command. This command has the following synopsis:

`[B8 xx 09 0A 40 00]`

The MMC responds to the **Get Payload Communication Timeout** command with the following reply:

`[BC xx 09 00 0A 40 00 <payload timeout>]`

The `<payload timeout>` parameter is the payload communication timeout measured in hundreds of milliseconds. Thus, the payload communication timeout may vary from 0.1 to 25.5 seconds. The default value of the payload communication timeout is specified by the CFG_APP_SIPL_PAYLOAD_TIMEOUT Configuration Parameter.

Set Payload Communication Timeout Command

To change the payload communication timeout, the **Set Payload Communication Timeout** command is used:

`[B8 xx 0A 0A 40 00 <payload timeout>]`

Graceful Payload Reset

The MMC supports the Graceful Reboot option of the **FRU Control** command. On receiving such a command, the MMC sets the Graceful Reboot Request bit of the MMC status, sends a status update notification to the payload, and waits for the **Graceful Reset** command from the payload. If the MMC receives such a command before the payload communication timeout time, it sends the 0x00 completion code (Success) to the carrier controller. Otherwise, the 0xC3 completion code (Timeout) is sent.

The **Graceful Reset** command has the following synopsis:

`[B8 xx 11 0A 40 00]`

Note that the MMC does not reset the payload on receiving the **Graceful Reset** command or timeout. If the MMC participation is necessary, the payload must request the MMC to perform a payload reset.

The **Graceful Reset** command is also used to notify the MMC about the completion of the payload shutdown sequence (refer to “Payload Shutdown Timeout,” on page 60).

Payload Diagnostic Interrupt

The MMC supports the Issue Diagnostic Interrupt feature of the **FRU Control** command. The payload is notified about a diagnostic interrupt over the SIPL as described in “Get Status Command,” on page 56. The payload is expected to return diagnostic interrupt results before the payload communication timeout using the **Diagnostic Interrupt Results** command of the SIPL. This command has the following synopsis:

`[B8 xx 12 0A 40 00 <diagnostic interrupt return code>]`

If the payload responds before the payload communication timeout, the diagnostic interrupt return code is forwarded to the carrier controller as the completion code of the **FRU Control** command response. Otherwise, the 0xC3 completion code (Timeout) is returned.

Payload Shutdown Timeout

When the carrier controller commands the MMC to shut down the payload (i.e. sends the FRU Control (Quiesce) command), the MMC notifies the payload about it by asserting appropriate alert and sending an alert notification to the payload (refer to “Get Status Command,” on page 56). Upon receiving this notification, the payload software is expected to initiate the payload shutdown sequence. After performing this sequence, the payload should send the **Graceful Reset** command (refer to “Graceful Payload Reset,” on page 59) to the MMC over the payload interface to notify the MMC that the payload shutdown is complete.

To avoid deadlocks that may occur if the payload software does not respond, the MMC provides a special timeout for the payload shutdown sequence. If the payload does not send the Graceful Reset command within a definite period of time, the MMC assumes that the payload shutdown sequence is finished, and sends a Module Quiesced hot-swap event to the carrier controller.

In addition to the above, for AMCs that support ACPI (x86-based processor boards), the MMC toggles the ACPI power button, which may be acted on by ACPI-aware operating systems.

- “Get Payload Shutdown Timeout Command,” on page 60
- “Set Payload Shutdown Timeout Command,” on page 60

Get Payload Shutdown Timeout Command

The MMC supports reading of the payload shutdown timeout using the **Get Payload Shutdown Timeout** command. This command has the following synopsis:

```
[B8 xx 15 0A 40 00]
```

The MMC responds to the **Get Payload Shutdown Timeout** command with the following reply:

```
[BC xx 15 00 0A 40 00 <LSB byte of timeout> <MSB byte of timeout>]
```

The payload shutdown timeout is measured in hundreds of milliseconds and stored as a 2-byte integer. The default value of the payload shutdown timeout is specified by a dedicated Configuration Parameter.

Set Payload Shutdown Timeout Command

To change the payload shutdown timeout, the **Set Payload Shutdown Timeout** command is used:

```
[B8 xx 16 0A 40 00 <LSB byte of timeout> <MSB byte of timeout>]
```

Get Geographic Address Command

The MMC allows reading the geographic address of the module using the **Get Geographic Address** command, which has the following synopsis:

```
[B8 xx 2C 0A 40 00]
```

The MMC responds to the **Get IPMB Address** command with the following reply:

`[BC xx 2C 00 0A 40 00 <geographic address>]`

The `<geographic address>` parameter has the bit fields shown in Table 4-10, “The <geographic address> Parameter Bit Fields,” below.

Table 4-10: The <geographic address> Parameter Bit Fields

Bits	Name	Description
0-1	GA0 Signal	0 = GA0 is grounded 1 = GA0 is unconnected 3 = GA0 is pulled up
2-3	GA1 Signal	0 = GA1 is grounded 1 = GA1 is unconnected 3 = GA1 is pulled up
4-5	GA2 Signal	0 = GA2 is grounded 1 = GA2 is unconnected 3 = GA2 is pulled up
6-7	NA	Reserved

Firmware Upgrade Process

The MMC firmware supports a reliable field upgrade procedure compatible with the *HPM.1 Specification*. The key features of the firmware upgrade procedures are as follows:

- The upgrade can be performed over the serial debug/payload interface or over IPMB-L.
- The upgrade procedure is performed while the MMC firmware is online and operating normally.
- Upgrades of the firmware component are reliable. A failure in the download (error or interruption) does not disturb the MMC's ability to continue using the “old” firmware or its ability to restart the download process. Upgrades of the boot loader component are not reliable and may render the MMC non-functional in case of an incomplete upgrade.
- Upgrades of the firmware component are reversible. The MMC firmware automatically reverts back to the previous firmware if there is a problem when first running the new code and can be reverted manually using the HPM.1-defined **Manual Rollback** command. Upgrades of the boot loader component are not reversible.

HPM.1 Boot Loader

- The HPM.1 boot loader does not perform any upgrade actions
- The HPM.1 boot loader is able to boot either of two redundant copies of the MMC firmware in flash
- The HPM.1 boot loader is able to automatically rollback a failed copy of the MMC firmware and activate the backup one
- The HPM.1 boot loader can be upgraded in-field as an HPM.1-upgradeable component

HPM.1 Firmware Upgrade

The HPM.1 upgrade procedure is managed by a utility called the *upgrade agent*. The `ipmitool` utility is used as upgrade agent for upgrading the MMC firmware.

The upgrade agent communicates with the MMC firmware via serial interface or IPMB-L, and uses the ATCA commands that are described in the *HPM.1 Specification* for upgrading the firmware. Updated firmware is packed into a special image that has a format described in the *HPM.1 Specification*. That image is used by the upgrade agent to prepare and upgrade the MMC firmware. The HPM.1 upgrade procedure includes the following steps:

1. **Preparation step**. This step erases the region in the flash memory where a component will be written.
2. **Component upload step**. This step is designed to upload the component image via IPMB or a serial interface, and write it into the flash memory.
3. **Component activation step**. This step is designed to activate the previously upgraded component; for the firmware component, this step can be deferred until a later time.

The MMC firmware supports two upgradeable components: the firmware itself and the boot loader. In case of an unsuccessful firmware upgrade it is possible to roll back to the old firmware. This is not true for the boot loader.

Note: *Extreme caution should be exercised when upgrading the boot loader. There is no backup copy of the boot loader and if for any reason the boot loader upgrade procedure fails, the firmware becomes non-functional after reboot and must be reprogrammed over JTAG.*

Upgrade Utilities

The firmware upgrade procedure is performed using the upgrade agent utility, implementing the HPM.1 Upgrade Protocol and capable of programming custom firmware images into the flash memory of the MMC over a serial interface or IPMB-L. Any HPM.1-compatible Upgrade Agent can be used to upgrade the MMC firmware. It is recommended to use the `ipmitool` utility for these purposes. The `ipmitool` utility is available from Performance Technologies. Contact Performance Technologies Customer Support and Services for contact information.

The firmware image is supplied to the `ipmitool` utility in a single file called an HPM.1 upgrade image (for information about the format of HPM.1 upgrade images refer to the HPM.1 specification).

Detailed HPM.1 Upgrade Procedure

The following images are available from Performance Technologies:

- `hpm1fw.img` - this image contains the MMC firmware
- `hpm1boot.img` - this image contains the boot loader
- `hpm1all.img` - this image contains both the firmware and the boot loader

These images can be used to upgrade corresponding components of the IPMC: the firmware, the boot loader or both.

The following snapshot samples a command performing firmware upgrade from a Linux host over LAN/IPMB:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x7c -b 7 hpm upgrade
hpm1fw.img activate
PICMG HPM.1 Upgrade Agent 1.0:
Validating firmware image integrity...OK
```

```
Performing preparation stage...
     Services may be affected during upgrade. Do you with to continue? y/n y...
OK
     Target Product ID : 15
     Target Manufacturer ID: 1556
Performing upgrade stage:
     Upgrading AVR-AMCm F/W
     with Version:     Major: 1
                       Minor: 70
                       Aux: 000 000 000 000
     Writing firmware: 100 % completed
Performing activation stage:
Firmware upgrade procedure successful
```

IPMI Communication Utility (ipmitool)

The `ipmitool` utility is a Linux application that can be used for a wide range of tasks involving IPMI-based communications. The following topics describe the installation process and provide information on specific applications of this utility.

Note: *Contact Performance Technologies Customer Support and Services for an enhanced version of `ipmitool`. Besides the standard functionality, it supports the following vendor-specific enhancements, which are not available in the official release (as of version 1.8.9):*

- *Support for the serial IPMI interface (Terminal Mode)*
- *Some improvements in HPM.1 upgrade protocol implementation.*
- *Support for double bridging via LAN for accessing MMCs through the Shelf Manager and carrier IPMC.*

The enhanced version is available in binary form for Windows and in source form for Linux.

Building the ipmitool Utility

Build and install the `ipmitool` utility on a Linux host system using the following procedure:

1. Unpack the source tarball obtained from the secure Web site and change to the `ipmitool` directory:

   ```
   bash$ tar xzf <ipmitool_package_name>
   bash$ cd ipmitool
   ```

2. Run the `configure` script to prepare for the build. The `--prefix=<dir>` option can be used to specify the directory where the resulting files are installed. If not specified, `/usr/local` is used (in this case, the installation requires root privileges).

   ```
   bash$ ./configure --prefix=/home/user/ipmitool
   ```

3. Run the **`make install`** command to build and install the `ipmitool` utility.

   ```
   bash$ make install
   ```

Accessing an MMC with ipmitool

The available access methods that can be used to communicate with the MMC depend on the MMC firmware configuration and overall system setup. The most frequently used access methods are the following:

- Via an Ethernet connection to a Shelf Manager that is able to access via IPMB-0 the carrier IPMC managing the MMC. See “Accessing an MMC via a Shelf Manager,” on page 64.

  This access method can be used from any Linux or Windows host that has an Ethernet connection to the Shelf Manager of the shelf in which the MMC is installed. In this access method, the `ipmitool` utility uses an Ethernet connection to the Shelf Manager to double bridge IPMI requests to the MMC over IPMB-0 and IPMB-L.
- Via the serial debug or serial payload interface of the MMC. See “Accessing an MMC via a Serial Interface,” on page 65.

  This access method can be used from any Linux or Windows host that has a serial connection with the MMC’s serial debug or serial payload interfaces. In this access method, the `ipmitool` utility uses a serial interface to directly access the MMC.

Accessing an MMC via a Shelf Manager

To access the MMC using an Ethernet connection to a Shelf Manager, the following parameters should be specified in the command line of the `ipmitool` utility:

`-I lan`

This command line parameter instructs the `ipmitool` utility to use Ethernet for communications with the MMC.

`-H <Shelf Manager IP>`

This command line parameter specifies the IP address of the Shelf Manager.

`-T <carrier IPMC address>`

This command line parameter specifies the remote transit address (IPMB-0 address of the carrier IPMC) to which requests should be bridged by the Shelf Manager.

`-B 0`

This command line parameter specifies the remote transit channel (with 0 designating IPMB-0) to which requests should be bridged by the Shelf Manager.

`-t <MMC address>`

This command line parameter specifies the remote target address (IPMB-L address of the MMC) to which requests should be bridged by the carrier IPMC.

`-b 7`

This command line parameter specifies the remote target channel (with 7 designating IPMB-L) to which requests should be bridged by the carrier IPMC.

`-A <authtype>`

This command line parameter forces the `ipmitool` to use a specific authentication type, which must, of course, be supported by the Shelf Manager.

For example, to fetch and print Sensor Device Records of an MMC at IPMB-L address `0x72` via a Shelf Manager with the IP address `192.168.0.2`, and a carrier IPMC at IPMB-0 address `0x82`, the following command line should be used:

```
# ipmitool –I lan –H 192.168.0.2 –T 0x82 –B 0 –t 0x72 –b 7 –A none sdr
```

Accessing an MMC via a Serial Interface

The following `ipmitool` command line parameters are used for communicating with the MMC via a serial interface:

```
-I serial-terminal
```

This command line parameter instructs the `ipmitool` utility to use the serial interface for communications with the MMC.

```
-D <dev[:baudrate]>
```

This command line parameter specifies the serial device and baud rate settings to use. For Linux hosts, the serial device is the system path to the device node (e.g. **/dev/ttyS0**). For the Cygwin-flavor of the `ipmitool` utility, Windows serial device names are translated as follows: the COM1 device name is mapped to **/dev/ttyS0**, COM2 is mapped to **/dev/ttyS1** and so on.

The supported baud rates are: 2400, 9600, 19200, 38400, 57600, and 115200.

For example, to fetch and print Sensor Device Records of an MMC via a serial interface connection with a baud rate of 9600, the following command line should be used:

```
# ipmitool –I serial-terminal –D /dev/ttyS0:9600 sdr
```

Using ipmitool for HPM.1 Upgrades

The `ipmitool` utility has built-in HPM.1 upgrade functionality and can be used as an upgrade agent. To be able to send HPM.1 commands to the MMC, the proper connection options should be specified in the `ipmitool` command line.

See “Accessing an MMC with ipmitool,” on page 64 for the list of available `ipmitool` command line connection options.

HPM.1 Commands

The `ipmitool` utility supports the following HPM.1 commands, which are described on the following pages:

- “targetcap,” on page 66
- “compprop,” on page 67
- “upgrade,” on page 68
- “activate,” on page 69
- “rollback,” on page 69
- “rollbackstatus,” on page 69

targetcap

Get the target upgrade capabilities. This command can be used to find out the upgrade capabilities of an MMC.

```
ipmitool hpm targetcap
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm targetcap
PICMG HPM.1 Upgrade Agent 1.0:
TARGET UPGRADE CAPABILITIES
------------------------------
HPM.1 version.............0
Component 0 presence....[y]
Component 1 presence....[y]
Component 2 presence....[n]
Component 3 presence....[n]
Component 4 presence....[n]
Component 5 presence....[n]
Component 6 presence....[n]
Component 7 presence....[n]
Upgrade undesirable.....[n]
Aut rollback override...[n]
IPMC degraded...........[n]
Defered[1] activation......[y]
Service affected........[y]
Manual rollback.........[y]
Automatic rollback......[y]
Self test...............[n]
Upgrade timeout.........[100 sec]
Self test timeout.......[0 sec]
Rollback timeout........[5 sec]
Inaccessibility timeout.[5 sec]
```

1. “Defered” is misspelled in the `ipmitool` utility.

compprop

Get the specified component properties. This command can be used to find out component-specific properties.

```
ipmitool hpm compprop <id> <select>
```

The <id> parameter specifies the component whose properties are read; 0 corresponds to the firmware component and 1 corresponds to the boot loader component. The <select> parameter specifies the property that should be acquired. The properties are the following:

0 General properties

1 Current firmware version

2 Description string

3 Rollback firmware version

4 Deferred firmware version

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm compprop 0 0
PICMG HPM.1 Upgrade Agent 1.0:
GENERAL PROPERTIES
-------------------------------
Payload cold reset req....[y]
Def. activation supported.[y]
Comparison supported......[n]
Preparation supported.....[y]
Rollback supported........[y]
```

upgrade

Upgrade the firmware with the specified image. This command can be used to upgrade the firmware using a valid HPM.1 image.

```
ipmitool hpm upgrade <file> [activate]
```

The `<file>` parameter specifies the name of the HPM.1 upgrade image. If the `[activate]` parameter is specified, the upgraded firmware is activated just after the upgrade procedure. In the other case, an additional command should be issued to activate the firmware.

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm upgrade
hpm1fw.img
Validating firmware image integrity...OK
Performing preparation stage...
     Services may be affected during upgrade. Do you wish to continue? y/n y
OK
     Target Product ID     : 15
     Target Manufacturer ID: 1556
Performing upgrade stage:
     Upgrading AVR-AMCm F/W
     with Version: Major: 0
                   Minor: 5
                   Aux  : 000 000 000 000
     Writing firmware: 100 % completed
```

activate

Activate the newly uploaded firmware. This command can be used for activating the newly uploaded firmware if there was no activate parameter passed to the upgrade command.

```
ipmitool hpm activate
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm activate
PICMG HPM.1 Upgrade Agent 1.0:
```

rollback

Perform a manual rollback on the IPM controller. This command can be used to roll back from the newly uploaded firmware to the old one.

```
ipmitool hpm rollback
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm rollback
PICMG HPM.1 Upgrade Agent 1.0:
```

rollbackstatus

Query the rollback status. This command can be used to query the firmware on the IPMC about whether a rollback event has occurred.

```
ipmitool hpm rollbackstatus
```

Example:

```
ipmitool -I lan -H 192.168.0.2 -A none -T 0x82 -B 0 -t 0x74 -b 7 hpm rollback-
status
PICMG HPM.1 Upgrade Agent 1.0:
Rollback occured[1] on component mask: 0x01
```

1. “occured” is misspelled in the `ipmitool` utility.

Chapter 5

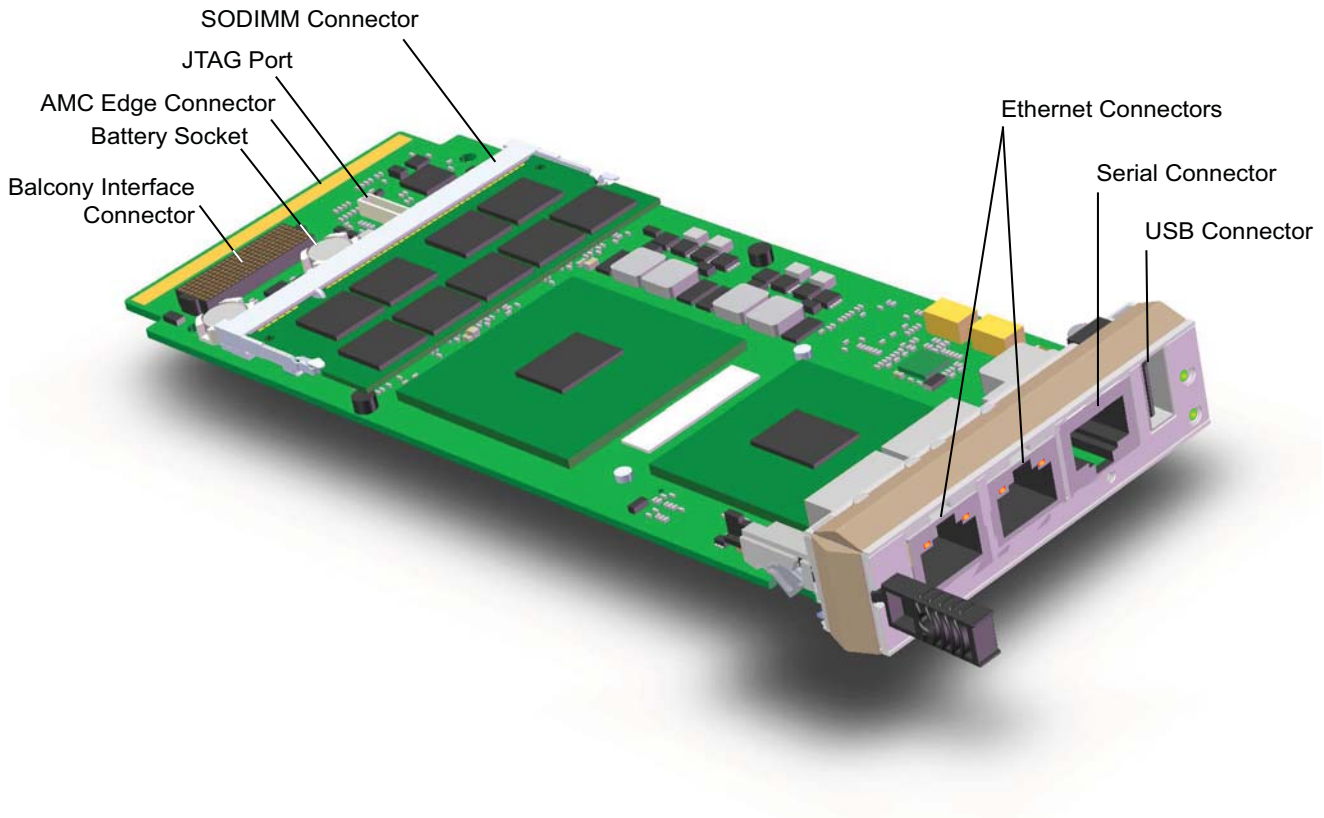
Connectors

As shown in Figure 5-1, “Connector Locations,” on page 71, the AMC121 includes several connectors to interface with application-specific devices. A brief description of each connector is given in Table 5-1. A detailed description and pinout for each connector is given in the following topics.

Table 5-1: Connector Assignments

Function	Location
AdvancedMC Card Edge Connector	Card Edge
Balcony Interface Connector	Internal
COM1 Serial Port	Front Panel
DDR SDRAM Connector	Internal
Ethernet Connectors	Front Panel
USB Connector	Front Panel

Figure 5-1: Connector Locations



Note: *Shown without balcony board for illustrative purposes only. Do not attempt to remove the balcony board from the AMC121. Doing so will void your warranty.*

AdvancedMC Card Edge Connector

The AdvancedMC Connector provides the electrical interface between the AMC121 and the carrier. The AdvancedMC connector is fixed to the carrier and the card edge interface at the back of the AMC121 plugs into it. There are different styles of connectors for the different types of AdvancedMC bays and for different levels of connectivity. The card edge interface on the AMC121 is compatible with the extended, 170 pin B+ style connector found on Performance Technologies' AMP5070 MicroTCA Platform.

Besides power and ground, the AMC121 card edge interface routes two SATA channels, PCI Express bus, dual SerDes 1Gb Ethernet channels and IPMI to the AdvancedMC connector.

See Table 5-2, “AMC Connector B+ footprint Pinout,” on page 73, for pin definitions and Figure 5-1 above for the location.

Table 5-2: AMC Connector B+ footprint Pinout

Slot Layer B				Slot Layer B			
Pin No.	Signal	Pin No.	Signal	Pin No.	Signal	Pin No.	Signal
B85	GND	B86	GND	B42	MB_PWR	B129	MB_Tx15-
B84	MB_PWR	B87	PCIE 4 RXN	B41	MB_ENABLE#	B130	MB_Tx15+
B83	MB_PS0#	B88	PCIE 4 RXP	B40	GND	B131	GND
B82	GND	B89	GND	B39	SATA 2 RXN	B132	MB_Rx15-
B81	MB_FCLKA-	B90	PCIE 4 TXN	B38	SATA 2 RXP	B133	MB_Rx15+
B80	MB_FCLKA+	B91	PCIE 4 TXP	B37	GND	B134	GND
B79	GND	B92	GND	B36	SATA 2 TXN	B135	MB_TCLKC-
B78	MB_TCLKB-	B93	PCIE 5 RXN	B35	SATA 2 TXP	B136	MB_TCLKC+
B77	MB_TCLKB+	B94	PCIE 5 RXP	B34	GND	B137	GND
B76	GND	B95	GND	B33	SATA 1 RXN	B138	MB_TCLKD-
B75	MB_TCLKA-	B96	PCIE 5 TXN	B32	SATA 1 RXP	B139	MB_TCLKD+
B74	MB_TCLKA+	B97	PCIE 5 TXP	B31	GND	B140	GND
B73	GND	B98	GND	B30	SATA 1 TXN	B141	MB_Tx17-
B72	MB_PWR	B99	PCIE 6 RXN	B29	SATA 1 TXP	B142	MB_Tx17+
B71	MB_SDA_L	B100	PCIE 6 RXP	B28	GND	B143	GND
B70	GND	B101	GND	B27	MB_PWR	B144	MB_Rx17-
B69	PCIE 3 RXN	B102	PCIE 6 TXN	B26	MB_GA2	B145	MB_Rx17+
B68	PCIE 3 RXP	B103	PCIE 6TXP	B25	GND	B146	GND
B67	GND	B104	GND	B24	GIGE 2 RXN	B147	MB_Tx18-
B66	PCIE 3 TXN	B105	PCIE 7 RXN	B23	GIGE 2 RXP	B148	MB_Tx18+
B65	PCIE 3 TXP	B106	PCIE 7 RXP	B22	GND	B149	GND
B64	GND	B107	GND	B21	GIGE 2 TXN	B150	MB_Rx18-
B63	PCIE 2 RXN	B108	PCIE 7 TXN	B20	GIGE 2 TXP	B151	MB_Rx18+
B62	PCIE 2 RXP	B109	PCIE 7 TXP	B19	GND	B152	GND
B61	GND	B110	GND	B18	MB_PWR	B153	MB_Tx19-
B60	PCIE 2 TXN	B111	MB_Tx12-	B17	MB_GA1	B154	MB_Tx19+
B59	PCIE 2 TXP	B112	MB_Tx12+	B16	GND	B155	GND
B58	GND	B113	GND	B15	GIGE 1 RXN	B156	MB_Rx19-
B57	MB_PWR	B114	MB_Rx12-	B14	GIGE 1 RXP	B157	MB_Rx19+
B56	MB_SCL_L	B115	MB_Rx12+	B13	GND	B158	GND
B55	GND	B116	GND	B12	GIGE 1 TXN	B159	MB_Tx20-
B54	PCIE 1 RXN	B117	MB_Tx13-	B11	GIGE 1 TXP	B160	MB_Tx20+
B53	PCIE 1 RXP	B118	MB_Tx13+	B10	GND	B161	GND
B52	GND	B119	GND	B9	MB_PWR	B162	MB_Rx20-
B51	PCIE 1 TXN	B120	MB_Rx13-	B8	MB_RSRVD8	B163	MB_Rx20+
B50	PCIE 1 TXP	B121	MB_Rx13+	B7	GND	B164	GND
B49	GND	B122	GND	B6	MB_RSRVD6	B165	MB_TCK
B48	PCIE 0 TXN	B123	MB_Tx14-	B5	MB_GA0	B166	MB_TMS
B47	PCIE 0 RXP	B124	MB_Tx14+	B4	MB_MP	B167	MB_TRST#
B46	GND	B125	GND	B3	MB_PS1#	B168	MB_TDO
B45	PCIE 0 TXN	B126	MB_Rx14-	B2	MB_PWR	B169	MB_TDI
B44	PCIE 0 TXP	B127	MB_Rx14+	B1	GND	B170	GND
B43	GND	B128	GND				

Front Panel Connectors

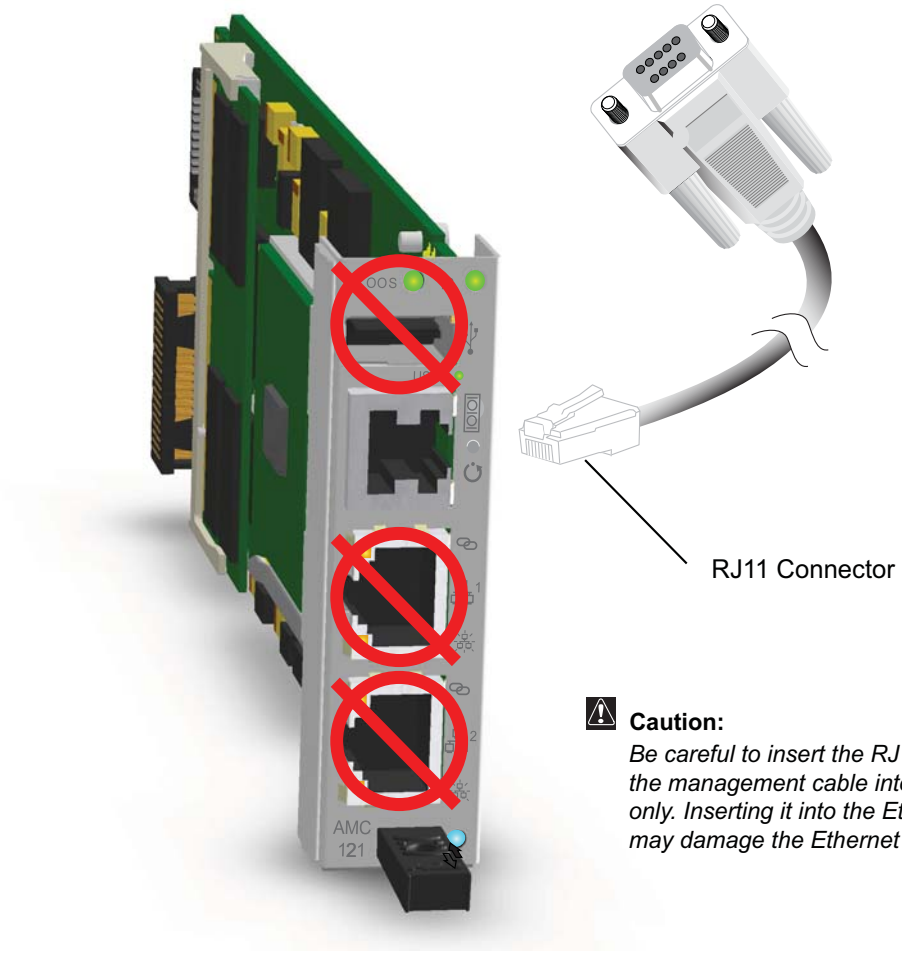
COM1 Serial Port

A 6-pin, RJ11 connector provides the COM1 interface on the AMC121's front panel. See Table 5-3, "COM1 Serial Port Pinout," for pin definitions and Figure 5-1, “Connector Locations,” on page 71, for connector identification. Also see “Serial Cables” on page 77.

Table 5-3: COM1 Serial Port Pinout

Pin#	Function	Pin#	Function
1	NC	5	GND
2	GND	6	NC
3	MMC_RXD		
4	MMC_TXD		

Figure 5-2: RJ11 Cable Connection



Caution:
Be careful to insert the RJ11 connector on the management cable into the Serial port only. Inserting it into the Ethernet connector may damage the Ethernet connector pins.

Ethernet Connectors

Two RJ45 connectors on the AMC121's front panel provide two 1000 Mbps (1000Base-T) Ethernet channels. Two bicolor LEDs are located inside each RJ45 connector:

- Front panel ENET link
- Front panel ENET activity

See the topic “LED Indicators” on page 27, for more information. See Table 5-4, “Ethernet Connectors Pinout,” for pin definitions and Figure 5-1, “Connector Locations,” on page 71, for connector identification.

Caution:
Insert only RJ45 connectors into the Ethernet connector. Other connectors may damage the Ethernet connector pins.

Table 5-4: Ethernet Connectors Pinout

Pin	Signal Name
1	MD0+
2	MD0-
3	MD1+
4	MD2+
5	MD2-
6	MD1-
7	MD3+
8	MD3-
MH1	NC
MH2	NC

USB Connector

A 4-pin USB 2.0 Port 0 Interface connector is available on the AMC121's front panel. See Table 5-5, “USB Connector Pinout,” for pin definitions and Figure 5-1, “Connector Locations,” on page 71, for connector identification.

Table 5-5: USB Connector Pinout

Pin#	Function
1	+5V Fused
2	DATA-
3	DATA+
4	GND

Internal Connectors

DDR SDRAM Connector

A 90°, 200-pin connector accommodates a 1.8V, 200-pin, PC2-3200 DDR SDRAM Registered SDRAM used for system memory. See Figure 5-1, “Connector Locations,” on page 71, for connector identification. For more information about system memory, see the topic “Memory Configuration” on page 36.

Memory is not a field serviceable item. Return the module to Performance Technologies for memory replacement. See “Return Merchandise Authorization (RMA)” on page 17 for more information about returning merchandise.

Balcony Interface Connector

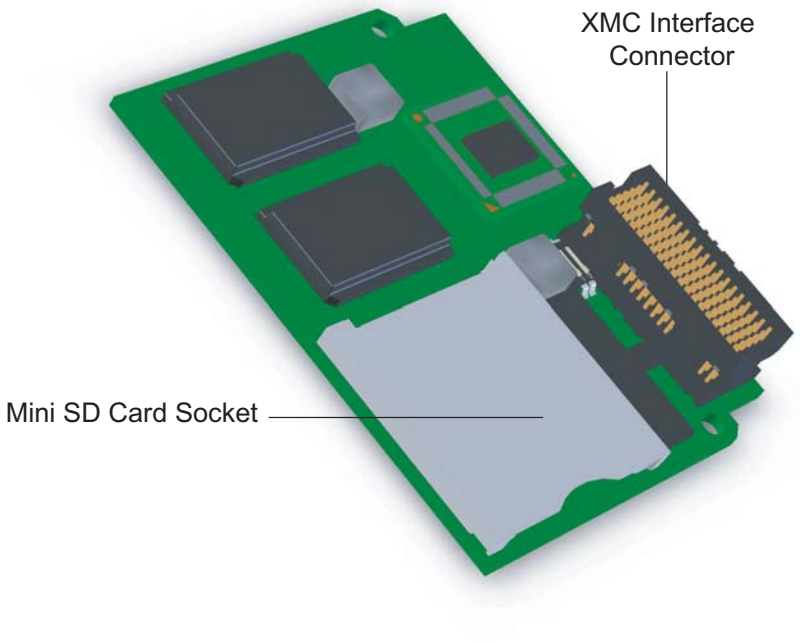
A 114-pin, pin-and-socket connector provides the interface between the base board and the balcony board. See Figure 2-4, “AMC121 with Balcony Board,” on page 32, Figure 5-1, “Connector Locations,” on page 71, and Figure 5-3, “Connector Locations (Balcony),” on page 77, for connector identification. See Table 5-6, “Balcony Interface Connector Pinout,” for pin definitions.

Caution:
Do not attempt to remove the balcony board from the AMC121. Doing so will void your warranty.

Table 5-6: Balcony Interface Connector Pinout

Pin #	A	B	C	D	E	F
19	LED1-	LED2-	RSVD	LED4-	LED3-	LPC_RST-
18	GND	ITP_TMS	RSVD	GND	E4_TFC_LED	LPC_FRAME-
17	ENET2C_P	ENET2C_N	SIO_GPIO	ENET1C_P	ENET1C_N	LPC_LAD3
16	GND	GND	LED5-	ITP_TDO	GND	RESET_RTN
15	ENET2D_P	ENET2D_N	RSVD	ENET1D_P	ENET1D_N	+5V
14	GND	ITP_DBREQ	USB2_N	GND	E4_LNK_LED	RESET-
13	ENET2A_P	ENET2A_N	+3.3V MGT	ENET1A_P	ENET1A_N	+5V
12	GND	GND	USB2_P	ITP_TDI	GND	BALC_PRES-
11	ENET2B_P	ENET2B_N	RSVD	ENET1B_P	ENET1B_N	+5V
10	GND	ITP_DBRDY	PYLD_TDO	GND	E3_TFC_LED	SCL
9	PCIE_CLK_P	PCIE_CLK_N	RSVD	SDA	LED0-	+5V
8	C_GND	GND	PAL_TDO	ITP_TRST-	GND	+2.5V
7	PCIE2_RXP2	PCIE2_RXN2	+3.3V	PCIE2_RXP3	PCIE2_RXN3	+3.3V
6	C_GND	GND	PYLD_TMS	GND	E3_LNK_LED	+2.5V
5	PCIE2_RXP0	PCIE2_RXN0	+3.3V	PCIE2_RXP1	PCIE2_RXN1	+3.3V
4	C_GND	GND	PYLD_TCK	ITP_TCK	GND	LED6-
3	PCIE2_TXP2	PCIE2_TXN2	+3.3V	PCIE2_TXN3	PCIE2_TXP3	+3.3V
2	C_GND	GND	PYLD_TRST-	GND	ITP_RST-	LED7-
1	PCIE2_TXP0	PCIE2_TXN0	+3.3V	PCIE2_TXP1	PCIE2_TXN1	+3.3V

Figure 5-3: Connector Locations (Balcony)



Note: *Balcony board shown separately for illustrative purposes only. Do not attempt to remove the balcony board from the AMC121. Doing so will void your warranty.*

Cables

Serial Cables

The front panel RJ11 serial connector may be used to access the MMC Command Line Interface or the COM1 port (see “COM1 Serial Port” on page 74). Some shelf managers require a DB-9 connector for this purpose. The serial cable provides a DTE connection (RS-232 levels), allowing connection to a modem (DCE) without the need of a null modem. A null modem (DB-9F to DB-9F) allows connection to a terminal or PC (DTE) directly.

A male RJ11 to female DB-9 management cable requires the following parts:

- Male RJ11 connector
- High quality cable, such as Category 5
- Female DB-9 connector

Table 5-7, “Management Cable Pinout,” on page 78, shows the required connections. The male DB-9 connector provides a loopback between DTR and DSR and a loopback between RTS and CTS.

Caution:
Be careful to insert the RJ11 connector on this cable into the serial port only. Inserting it into the Ethernet connector may damage the Ethernet connector pins.

Table 5-7: Management Cable Pinout

DB-9 Pin	RJ11	Serial Protocol Name (EIA574 Mnemonic)
1	N/C	N/C
2	3	RXD (104)
3	4	TXD (103)
4	N/C	DTR (108)
5	2, 5	GND (102)
6	N/C	DSR (107)
7	-	RTS (105)
8	-	CTS (106)
9	-	N/C

This chapter discusses the various reset types and reset sources on the AMC121. Because many embedded systems have different requirements for board reset functions, the incorporation of this sub-system on the AMC121 has been designed to provide maximum flexibility.

Reset Types and Sources

The AMC121's four reset types are listed below. The sources for each reset type are detailed in the following topics.

- **Power On Reset**
- **Backend Power Down:** The backend logic is powered off. All on-board devices are reset.
- **Push Button Reset:** All on-board devices are reset
- **NMI:** Non-Maskable Interrupt. Though not a reset in the strict sense, an NMI can have the same effect as other resets.

Power On Reset

The AMC121 is held in reset until the PCI Express reference clock (FCLKA) source is determined. The AMC.1 R2.0 specification requires that FCLKA is e-keyed. The AMC121 is shipped from the factory configured for AMC.1 R2.0 e-keying of FCLKA.

AMC.1 R1.0 carriers do not e-key FCLKA. If the AMC121 does not come out of reset when powered on, it is likely that FCLKA is not configured properly for the specific carrier. Refer to “SW2-2 (Position 2) - FCLKA Configuration,” on page 40, for information on configuring FCLKA.

Backend Power Down Sources

Board Extraction

When the AMC121 is extracted from a carrier, the carrier hot swap controller unconditionally removes backend power from the AMC121 and holds it in reset.

General Reset Sources

Push-Button Reset

When the reset button on the front panel is pressed, the AMC121 resets itself.

Sources for push-button reset include:

- Front panel push-button reset switch (see Figure 2-1, “AMC121 Front Panel,” on page 21)
- Programmable watchdog timer

NMI\SMI\SERIRQ Sources

The Watchdog Timer

The watchdog timer can be programmed to generate a non-maskable interrupt or system management interrupt if it is not strobed within a given time-out period.

This chapter describes the electrical, environmental, and mechanical specifications of the AMC121.

Electrical and Environmental Specifications

The subsequent topics provide tables and illustrations showing the following electrical and environmental specifications:

- Absolute maximum ratings
- DC operating characteristics
- Battery backup characteristics

AMC121 Absolute Maximum Ratings

The values below are stress ratings only. Do not operate the AMC121 at these maximums. See the topic “DC Operating Characteristics” on page 82, for operating conditions.

Supply Voltage, Vcc12 (+12V):	10-14V
Supply Voltage, Vcc3 (+3.3V):	3.0-3.6V
Storage Temperature:	-40° to +85° C
Non-Condensing Relative Humidity:	<95% at 40° C

Operating Temperature

The operating temperature range is 0°C to 55°C. The AMC121 comes from the factory with an integrated heat sink for cooling the processor. The heat sink requires 300 LFM (linear feet per minute) of airflow. The maximum power dissipation of the CPU is dependent on the CPU installed.

Caution:
External airflow must be provided at all times during operation to avoid damaging the CPU module. Performance Technologies strongly recommends use of a card rack fan tray to supply the external airflow.

DC Operating Characteristics

Table 7-1 shows power consumption of an AMC121 with a dual core 1.5 GHz, 17 W Merom processor (L7400) with 2GB DDR2 400 SDRAM installed.

Table 7-1: Power Consumption with 1.5 GHz Processor

Voltage (VDC)	Maximum Power (W)
12V, (10 - 14V)	39.6W Max
3.30 V, (3.0 - 3.6V)	3.30 = 0.4W Max
Total Power	40W Total

Battery Backup Characteristics

The battery backup circuit on the AMC121 contains two ML621 manganese lithium batteries that are charged during normal operation and are used only when power is not applied to the board. The battery operates from -20°C to 60°C under normal operating conditions. Fully charged batteries can keep the battery-backed portions of the AMC121 powered for >60 days. For ensuring discharged batteries are restored to a fully charged state, ensure power is applied >30 hours.

Battery Replacement

Under normal operating conditions, it is not anticipated that the battery will require replacement during the life of the product. Each customer must evaluate their operating conditions to determine if a battery maintenance program is required as part of a regular maintenance cycle for their board.

There are two options in the event the battery must be replaced:

- Return the board to Performance Technologies to have the battery replaced
- Contact Performance Technologies to obtain a list of vendors of batteries approved for the product. You should also request detailed instructions for battery replacement in the field.

Note: *If you decide to replace the battery in the field, you are responsible for any damage that may occur to the board during battery replacement.*

Battery Voltage: 3 V

Battery Capacity: 10 mAh (5mAh x 2)

Electrochemical Construction: Manganese (ML series) lithium battery

Battery Socket Location: See Figure 5-1, “Connector Locations,” on page 71

Caution:
The AMC121 contains two manganese lithium batteries. There is a danger of explosion if the batteries are incorrectly replaced or handled. Do not disassemble or recharge the batteries. Do not dispose of the batteries in fire. When a battery is replaced, the same type or an equivalent type recommended by the manufacturer must be used. Used batteries must be disposed of according to the manufacturer's instructions.

AMC121 Reliability

Board MTBF = 653,948 per Bellcore SR-332 Issue 1

MTTR: 3 min

Mechanical Specifications

The AMC121 meets the PICMG AMC.0, R 2.0 specification for all mechanical parameters.

Mechanical dimensions are shown in Figure 7-1, “AMC121 Board Dimensions,” on page 83, and are outlined below.

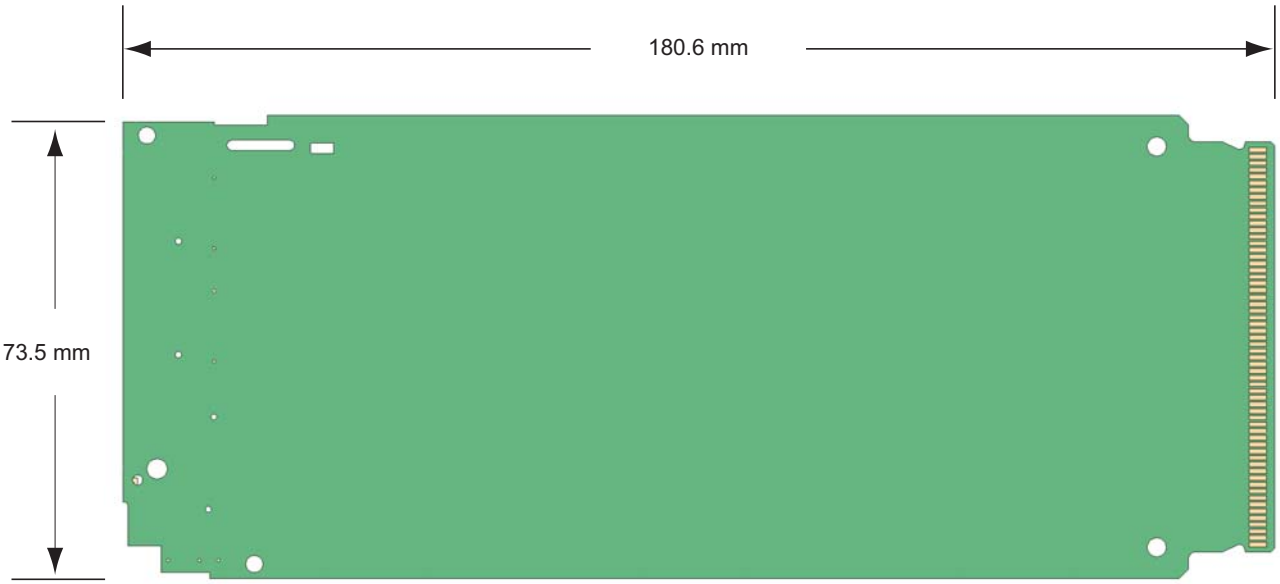
Board Length: 180.6 mm (7.11 in)

Board Width: 73.5 mm (2.89 in)

Board Height: 18.96 mm (0.75 in)

Board Weight: 0.25 kg (0.55 lb) with a 2 GB SDRAM loaded

Figure 7-1: AMC121 Board Dimensions



This chapter describes the thermal requirements to reliably operate an AMC121 processor module.

Thermal Requirements

The maximum processor die temperature allowed by the L7400 Core 2 Duo processor on the AMC121 is 100° C.

Caution:
To avoid damaging the CPU, do not exceed the maximum processor core temperature!

The maximum ambient air temperature required by the heat sink to maintain core temperature below the maximum is 55° C. The maximum ambient air temperature assumes airflow of 300 linear feet per minute past the heat sink.

Caution:
External airflow must be provided at all times during operation to avoid damaging the CPU. Performance Technologies strongly recommends use of a fan tray below the card rack to supply the external airflow.

Temperature Monitoring

Because reliable long-term operation of the AMC121 depends on maintaining proper temperature, Performance Technologies strongly recommends that you verify the operating temperature of the processor (core) in your final system configuration.

The Core 2 Duo L7400 processor incorporates an on-die thermal diode that can be used to monitor the processor's die temperature. While the MMC checks the die temperature of the processor for thermal monitoring, it relies on the Thermal Control Circuit (TCC) to manage the processor temperature.

Intel Thermal Monitor

The Intel thermal monitor controls the processor temperature by modulating the processor core clocks or by initiating an enhanced Intel SpeedStep technology transition when the processor reaches its maximum temperature. The AMC121 operates the thermal monitor in automatic mode so that the thermal management is transparent to normal board operation.

If the Intel thermal monitor fails, the host CPU generates a hardware signal THERMTRIP_L to immediately shut off power to the AMC121.

See the topic “Processor” on page 91 for more information on how the Intel Core 2 Duo processor thermal monitor functions.

Chapter 9

Agency Approvals

This chapter presents agency approval and certification information for the AMC121 Intel Core 2 Duo Processor AdvancedMC Module. Key topics in this chapter:

- "Network Equipment-Building System (NEBS) and European Telecommunications Standards Institute (ETSI)," on page 87
- "CE Certification," on page 87
- "EN55022 Radiated and Conducted Emissions," on page 88
- "EN300 386 Electromagnetic Compatibility (EMC)," on page 88
- "EN55024 Immunity," on page 88
- "Safety," on page 88
- "FCC (USA) Class A Notice," on page 88
- "Industry Canada Class A Notice," on page 89
- "Product Safety Information," on page 89
- "Compliance with RoHS and WEEE Directives," on page 90

Network Equipment-Building System (NEBS) and European Telecommunications Standards Institute (ETSI)

The product described in this manual is designed to meet NEBS Level 3 and ETSI Environmental Criteria:

- GR-63-CORE - *Network Equipment-Building System Requirements: Physical Protection*
- GR-1089-CORE - *Electromagnetic Compatibility and Electrical Safety - Generic Criteria for Network Telecommunications Equipment*

CE Certification

The product described in this manual meets the intent of the following European Union Directives:

- *EU 89/336/EEC Electromagnetic Compatibility Directive*, amended by 92/31/EEC, 93/68/EEC, 98/13/EEC, and 2004/108/EC
- *EU 72/23/EEC Low Voltage Directive*, amended by 93/68/EEC and 2006/95/EC

by meeting the applicable EU standards as outlined in the *Declaration of Conformance*. The *Declaration of Conformance* is available from Performance Technologies, or from your authorized distributor. Compliance will be demonstrated to the following specifications as listed in the *Official Journal of the European Communities*.

EN55022 Radiated and Conducted Emissions

EN300 386 Electromagnetic Compatibility (EMC)

EN55024 Immunity

EN61000-4-2	Electro-Static Discharge (ESD)
EN61000-4-3	Radiated Susceptibility
EN61000-4-4	Electrical Fast Transient Burst
EN61000-4-5	Surge Immunity
EN61000-4-6	Frequency Magnetic Fields
EN61000-4-11	Voltage Dips, Variations, and Short Interruptions

Safety

The product described in this manual meets the following safety regulations:

EN/IEC 60950	Safety Requirements for Information Technology Equipment
CB Scheme	CB Scheme Certificate and Report
UL60950	UL Recognized

FCC (USA) Class A Notice

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesired operation.

Note: *Modifications made to this device that are not approved by Performance Technologies, Inc. may void the authority granted to the user by the FCC to operate this equipment.*

Industry Canada Class A Notice

This Class A digital apparatus complies with Industry Canada's Equipment Standard for Digital Equipment (ICES-003).

Cet appareil numérique de la classe A est conforme à la norme NMB-003 du Canada.

Product Safety Information

Safety Precautions

Review the following precautions to avoid injury and prevent damage to this product, or any products to which it is connected. To avoid potential hazards, use the product only as specified.

Read all safety information provided in the component product user manuals and understand the precautions associated with safety symbols, written warnings, and cautions before accessing parts or locations within the unit. Save this document for future reference.

Caution:
To Avoid Burns: *If there is a heat sink on this module, it can get very hot during normal operation. To avoid burns, take extra care when removing the module from the chassis soon after shutdown. Wait a few minutes to allow the heat sink to cool down.*

Caution:
Handling the Module: *It is important to hold the module only by the front panel or PCB edges. Avoid touching any components unless necessary to service the product. Do not handle the heat sink, as this can adversely affect the thermal connection between the heat sink and the processor, and cause the processor to overheat under normal operating conditions.*

Caution:
To Avoid Electric Overload: *To avoid electrical hazards (heat, shock and/or fire hazard), do not make connections to terminals outside the range specified for that terminal. Refer to the product user manual for correct connections.*

Caution:
To Avoid the Risk of Electric Shock: *When supplying power to the system, always make connections to a grounded main. Always use a power cable with a grounded plug (third grounding pin). Do not operate in wet, damp, or condensing conditions.*

Caution:
System Airflow Requirements: *Platform components such as processor boards, Ethernet switches, etc., are designed to operate with external airflow. Components can be destroyed if they are operated without external airflow. Chassis fans normally provide external airflow when components are installed in compatible chassis. Filler panels must be installed over unused chassis slots so that airflow requirements are met. Please refer to the product data sheet for airflow requirements if you are installing components in custom chassis.*

Caution:
Do Not Operate Without Covers: *To avoid electric shock or fire hazard, do not operate this product with any removed enclosure covers or panels.*

Caution:
To Avoid the Risk of Electric Shock: *Do not operate in wet, damp, or condensing conditions.*

Caution:
Do Not Operate in an Explosive Atmosphere: *To avoid injury, fire hazard, or explosion, do not operate this product in an explosive atmosphere.*

Caution:
If Your System Has Multiple Power Supply Sources: *Disconnect all external power connections before servicing.*

Warning:
System power supplies must be replaced by qualified service personnel only.

Compliance with RoHS and WEEE Directives

In February 2003, the European Union issued *Directive 2002/95/EC* regarding the Restriction of the use of certain Hazardous Substances in electrical and electronic equipment (RoHS) and *Directive 2002/96/EC* on Waste Electrical and Electronic Equipment (WEEE).

This product is compliant with *Directive 2002/95/EC*. It may also fall under the *Directive 2002/96/EC*.

PT's complete position statements on the RoHS and WEEE Directives can be viewed on the Web at: http://pt.com/page/about-us/ehsms/.

Chapter 10

Data Sheet Reference

This chapter provides links to data sheets, standards, and specifications for the technology designed into the AMC121.

Processor

For more information about the Intel Core 2 Duo Processor (L7400), see the Intel Web site at:
http://www.intel.com/design/intarch/core2duo/index.htm?iid=ipp_embed+proc_core2duo&

The following are some useful application notes on the Intel Web site:

- Intel 64 and IA-32 Architectures Software Developer's Manuals
  http://www.intel.com/products/processor/manuals/index.htm
- Execute Disable Bit and Enterprise Security
  http://www.intel.com/technology/xdbit/
- AP-485 Intel Processor Identification and CPUID Instruction
  http://www.intel.com/Assets/PDF/appnote/241618.pdf

Chipset

The AMC121 incorporates the Intel 3100 chipset with integrated northbridge and southbridge.

More information on the Intel 3100 chipset may be found on Intel's Web site at:

http://www.intel.com/design/chipsets/embedded/
3100_coreduo.htm?iid=ipp_embed+chip_3100_coreduo&

Ethernet

The AMC edge connector high speed 1 / 2.5 Gigabit SerDes Ethernet is implemented on the AMC121 via the Broadcom BCM5708S. Refer to the following Web page for more information.

http://www.broadcom.com/collateral/pb/5708S-PB08-R.pdf

The front-panel gigabit Ethernet is implemented on the AMC121 via the Intel 82571EB GbE controller. Refer to the following Web page for more information:

http://www.intel.com/design/network/products/lan/controllers/82571eb.htm

Module Management Controller

The MMC is implemented with ATMEL's 8-bit microcontroller with 128 KB in-system programmable flash. For more information, the following document can be downloaded from the ATML Web site:

http://www.atmel.com/dyn/resources/prod_documents/doc2467.pdf

See the Intel IPMI home page for information concerning the Intelligent Platform Management Interface, including the Intelligent Platform Management Interface v1.5 Specification and the Intelligent Platform Management Interface Implementer's Guide:

http://developer.intel.com/design/servers/ipmi/spec.htm

I/O Controller

The following AMC121 functions reside in the Intel 3100 integrated chipset:

- Serial port controller (COM1)
- Real-time clock and CMOS memory
- Intelligent power management

Contact Intel Corp. for more information on the Intel 3100 integrated chipset:

http://www.intel.com/design/chipsets/embedded/3100_coreduo.htm?iid=ipp_embed+chip_3100_coreduo&

PICMG Specifications

The AMC121 is compliant with the following PICMG specifications:

- PICMG AMC.0, R 2.0 compliant
- IPMI v1.5 specification compliant

These specifications can be purchased from PICMG (PCI Industrial Computers Manufacturers Group). A short form specification in Adobe Acrobat format (PDF) is also available on PICMG's Web site at:

https://www.picmg.org

User Documentation

The latest Performance Technologies product information and manuals are available on the Performance Technologies Web site. BIOS and driver updates are also available from this site:

http://www.pt.com

Information specific to the AMC121 is available at this URL:

http://pt.com/content/amc121